AsahiKASEI MICRODEVICES

AK4497S

Sound Quality Oriented 32-Bit 2ch DAC

1. General Description

The AK4497S is a new generation Premium 32-bit 2ch DAC with VELVET SOUND™ technology, achieving low distortion characteristics and wide dynamic range. The OSR-Doubler technology establishes wide signal band, low power consumption and low distortion characteristics. Moreover, the AK4497S has six types of 32-bit digital filters, realizing simple and flexible sound tuning in wide range of applications. The AK4497S accepts up to 768 kHz PCM data and 22.4 MHz DSD data, suitable for a high-resolution audio source playback that are becoming widespread in network audios and USB-DACs.

Application: AV Receivers, CD/SACD player, Network Audio systems, USB DACs, USB Headphones, Sound Plates/Bars, Measurement equipment, Control systems, Public Address (PA), IC-Recorders, Bluetooth Headphones, HD Audio/Voice Conference Systems, Car Audio systems.

2. Features

- **THD+N: −117 dB (±2.8 Vpp), −113 dB (±3.75 Vpp)**
- **DR, S/N: 129 dB (±2.8 Vpp), 131 dB (±3.75 Vpp), 133 dB (Mono mode, ±3.75 Vpp)**
- **256 Times Over Sampling**
- **Audio I/F Format:**
  - **24/32-bit MSB Justified**
  - **16/20/24/32-bit LSB Justified**
  - **16/24/32-bit I^2S Compatible**
  - **TDM128/256/512**
  - **DSD64/128/256/512**
  - **External Digital Filter Interface (EXDF)**
- **Sampling Frequency:**
  PCM : 30 kHz to 768 kHz
  EXDF : 384 kHz, 768 kHz
  DSD : 2.8 MHz, 5.6 MHz, 11.2 MHz, 22.4 MHz
- **32-bit 8x Digital Filter**
  - **Short Delay Sharp Roll-off, Group Delay = 6.0/fs,**
  - **Short Delay Slow Roll-off, Group Delay = 5.0/fs**
  - **Sharp Roll-off**
  - **Slow Roll-off**
  - **Low Dispersion Short Delay Filter, Group Delay = 10.0/fs**
  - **Super Slow Roll-off**
- **DSD filter**
  - **Filter1 (fc = 39 kHz, DSD64 mode), Filter2 (fc = 76 kHz, DSD64 mode)**
- **Digital De-emphasis for 32 kHz, 44.1 kHz, and 48 kHz sampling**
- **Soft Mute**
- **Digital Attenuator (0 dB to −127 dB/ 0.5 dB step, and Mute)**
- **Mono mode**
- **Master Clock (PCM mode)**

fs = 30 kHz to 32 kHz	**:**	**256fs, 384fs, 512fs, 768fs, 1152fs**
fs = 32 kHz to 54 kHz	**:**	**256fs, 384fs, 512fs, 768fs**
fs = 54 kHz to 108 kHz	**:**	**256fs, 384fs**
fs = 108 kHz to 216 kHz	**:**	**128fs, 192fs**
fs = 216 kHz to 388 kHz	**:**	**32fs, 48fs, 64fs, 96fs**
fs = 388 kHz to 776 kHz	**:**	**16fs, 32fs, 48fs, 64fs**

- **Operation Control: Register Control by 3-wire Serial or I²C-bus, Pin Control**
- **Digital Input Level: CMOS**
- **Power Supply:**
  - **Using Internal LDO for Digital Core (DVDD)**
    - **AVDD, TVDD: 3.0 to 3.6 V**
    - **VDDL, VDDR: 4.75 to 5.25 V**
  - **Using External Supply for Digital Core (DVDD)**
    - **AVDD, TVDD: DVDD to 3.6 V**
    - **DVDD: 1.7 to 1.98 V**
    - **VDDL, VDDR: 4.75 to 5.25 V**
- **Operational Temperature: −40 to 105 °C**
- **Package: 64-pin HTQFP (Mold Size 10 mm × 10 mm, Pin Pitch 0.5 mm)**

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4. Block Diagram and Functions

4.1. Block Diagram

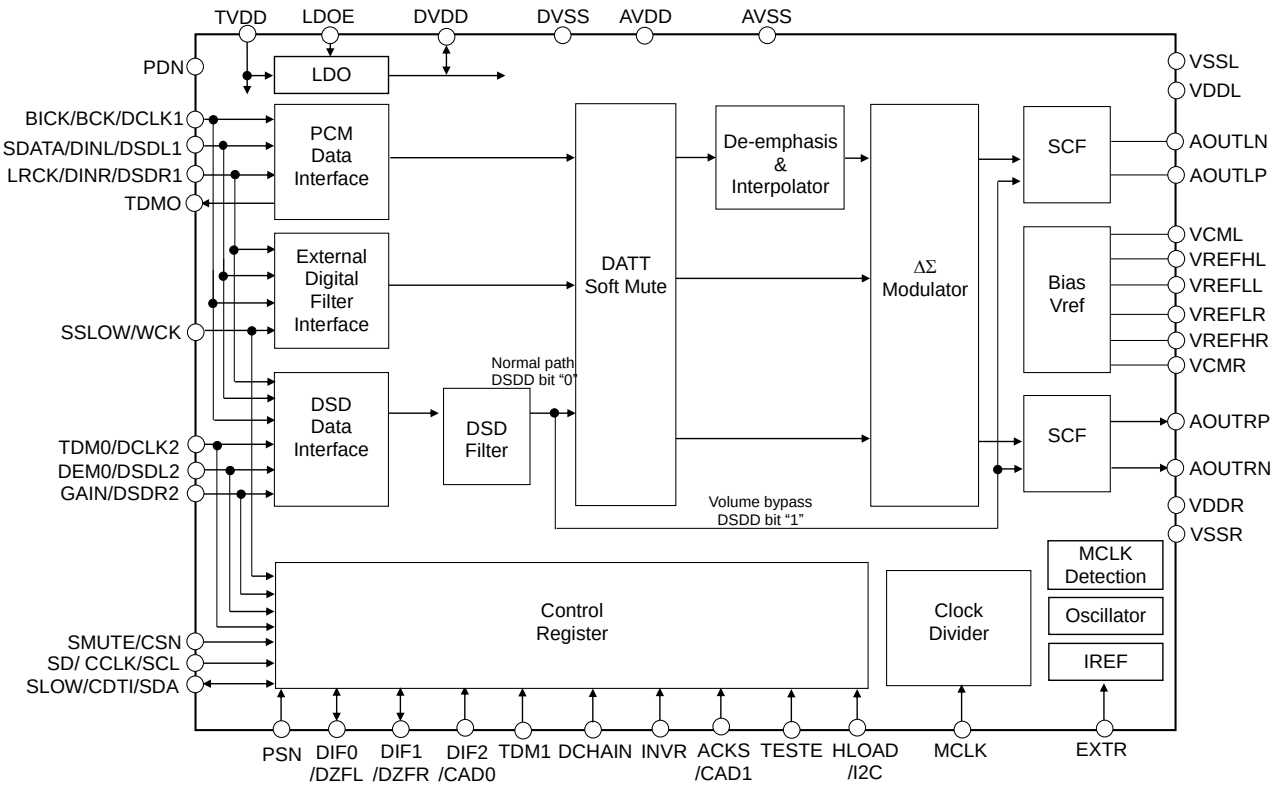


Figure 1. Block Diagram

4.2. Block Functions

Block	Function
PCM Data Interface	Receives serial data input to the SDATA pin in synchronization with LRCK and BICK, and converts it to parallel data for internal use. In TDM256 and TDM512 modes, outputs TDM data for daisy-chain connection.
External Digital Filter Interface	Receives serial data from an external filter input to the DINL and DINR pins in synchronization with WCK and BCK, and converts it to parallel data.
DSD Data Interface	Receives 1-bit data input to the DSDLx and DSDRx (x = 1 or 2) pins in synchronization with DCLK.
DSD Filter	FIR filter that reduces high frequency noise of DSD input data
DATT, Soft Mute	Applies Digital Attenuation and Soft Mute process to the input data.
De-emphasis & Interpolator	Applies De-emphasis and oversampling to the input data.
ΔΣ Modulator	A third-order digital ΔΣ modulator that applies noise shaping to the input data.
SCF	A Switched Capacitor Filter that converts output of ΔΣ Modulator into analog signal.
Control Register	Registers that hold the settings for various operating modes. The control register is accessed through a 3-wire serial interface (CSN, CCLK, CDTI) or an I^2C-bus (SCL, SDA).
Clock Divider	Divides the master clock (MCLK) to create the clocks required for internal processing.
MCLK Detection	Monitors whether MCLK input is present and powers off the D/A conversion sections when MCLK stops.
Bias, Vref	Generates common voltage VCML/R from the reference voltages VREFHL/R and VREFLL/R.
Oscillator	Generates reference clock for judging the LRCK and WCK frequency.
IREF	Generates reference current from reference voltage and external resistor.
LDO	Provides 1.8 V supply generated from TVDD to the internal digital circuitry.

5. Pin Configurations and Functions

5.1. Pin Configurations

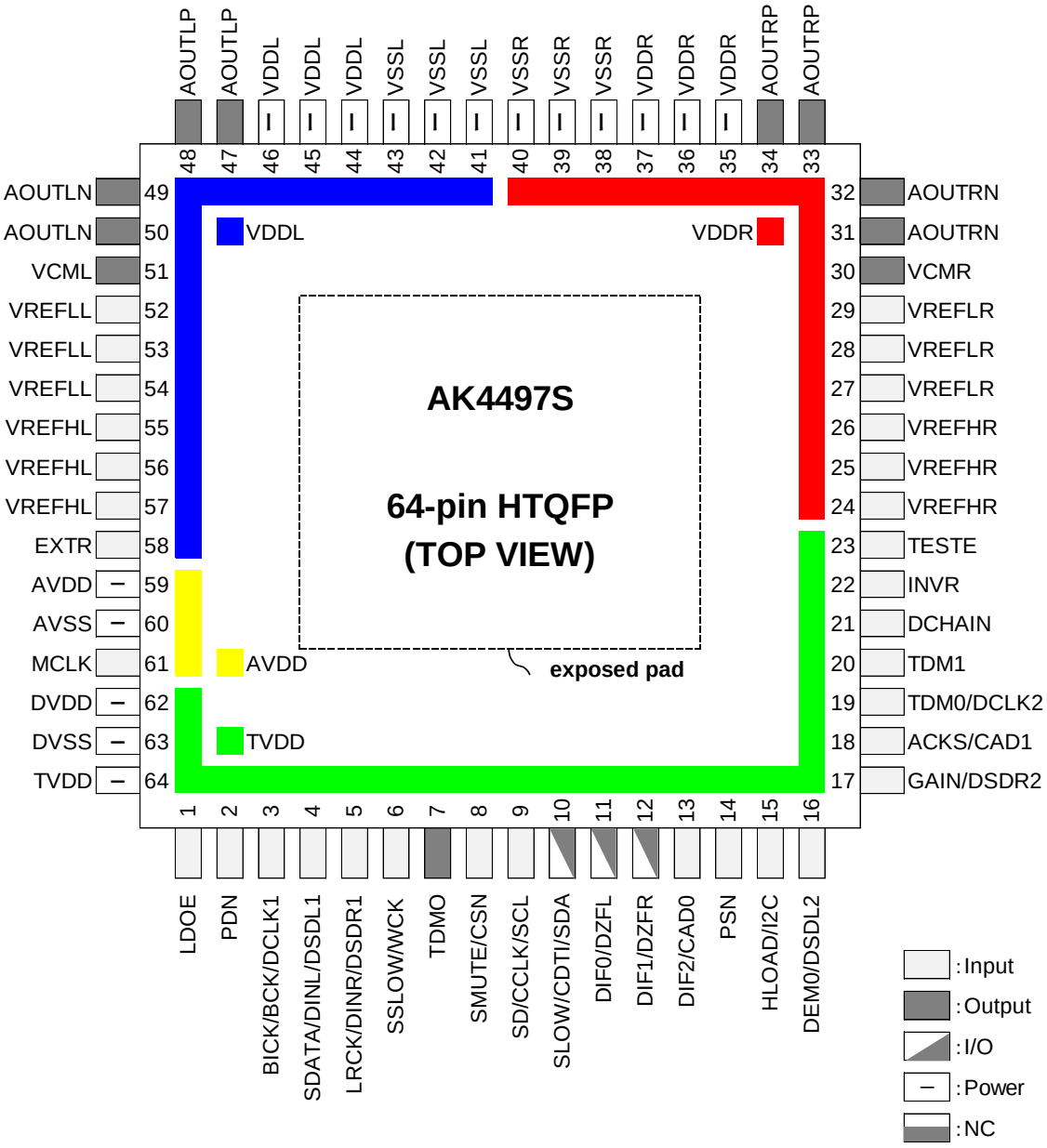


Figure 2. Pin Configurations

The exposed pad on the bottom surface of the package must be connected to AVSS.

5.2.

5.3. Pin Functions

No.	Pin Name	I/O	Protection Diode	Function	Power Down State
1	LDOE	I	TVDD DVSS	Internal LDO Enable Pin. “L”: Disable, “H”: Enable	Hi-Z
2	PDN	I	TVDD DVSS	Power Down Pin When PDN pin is “L”, the AK4497S is in power down mode and is held in reset. The AK4497S must always be reset upon power-up.	Hi-Z (PDN = “L”)
3	BICK	I	TVDD DVSS	Audio Serial Data Clock Pin in PCM mode	Hi-Z
	BCK	I		Audio Serial Data Clock Pin in EXDF mode	
	DCLK1	I		DSD Clock Pin in DSD mode (DSDPATH bit = “1”)	
4	SDATA	I	TVDD DVSS	Audio Serial Data Input Pin in PCM mode	Hi-Z
	DINL	I		Lch Audio Serial Data Input Pin in EXDF mode	
	DSDL1	I		DSD Lch Data Input Pin in DSD mode (DSDPATH bit = “1”)	
5	LRCK	I	TVDD DVSS	L/R Clock Pin in PCM mode	Hi-Z
	DINR	I		Rch Audio Serial Data Input Pin in EXDF mode	
	DSDR1	I		DSD Rch Data Input Pin in DSD mode (DSDPATH bit = “1”)	
6	SSLOW	I	TVDD DVSS	Digital Filter Select Pin in Pin Control mode	Hi-Z
	WCK	I		Word Clock Input Pin in EXDF mode	
7	TDMO	O	TVDD DVSS	Audio Serial Data Output Pin in Daisy Chain mode (Internal pull-down pin)	Pull-down to DVSS (typ. 100 kΩ)
8	SMUTE	I	TVDD DVSS	Soft Mute Enable Pin When this pin is changed to “H”, soft mute cycle is initiated. When returning “L”, the output mute releases.	Hi-Z
	CSN	I		Chip Select Pin in 3-wire Serial Control mode	
9	SD	I	– DVSS	Digital Filter Select Pin in Pin Control mode	Hi-Z
	CCLK	I		Clock Pin in Register in 3-wire Serial Control mode	
	SCL	I		Clock Input Pin in I^2C-bus Control mode	
10	SLOW	I	– DVSS	Digital Filter Select Pin in Pin Control mode	Hi-Z
	CDTI	I		Control Data Input Pin in 3-wire Serial Control mode	
	SDA	I/O		Control Data Input Pin in I^2C-bus Control mode	
11	DIF0	I	TVDD DVSS	Digital Input Format 0 Pin in Pin Control mode (Internal pull-down pin)	Pull-down to DVSS (typ. 100 kΩ)
	DZFL	O		Lch Zero Input Detect Pin in Register Control mode (Internal pull-down pin)	
12	DIF1	I	TVDD DVSS	Digital Input Format 1 Pin in Pin Control mode (Internal pull-down pin)	Pull-down to DVSS (typ. 100 kΩ)
	DZFR	O		Rch Zero Input Detect Pin in Register Control mode (Internal pull-down pin)	
13	DIF2	I	TVDD DVSS	Digital Input Format 2 Pin in Pin Control mode	Hi-Z
	CAD0	I		Chip Address 0 Pin in Register Control mode	

No.	Pin Name	I/O	Protection Diode	Function	Power Down State
14	PSN	I	TVDD DVSS	Control Mode select Pin (Internal pull-up pin) “L”: Register Control mode, “H”: Pin Control mode	Pull-up to TVDD (typ. 100 kΩ)
15	HLOAD	I	TVDD DVSS	Heavy Load mode Enable Pin in Pin Control mode	Hi-Z
	I2C	I		Register Interface Select Pin in Register Control mode “L”: 3-wire Serial Control mode, “H”: I^{2}C-bus Control mode	
16	DEM0	I	TVDD DVSS	De-emphasis Enable 0 Pin in Pin Control mode	Hi-Z
	DSDL2	I		DSD Lch Data Input Pin in DSD mode (DSDPATH bit = “0”)	
17	GAIN	I	TVDD DVSS	Output Gain Control Pin in Pin Control mode (+2.5 dB)	Hi-Z
	DSDR2	I		DSD Rch Data Input Pin in DSD mode (DSDPATH bit = “0”)	
18	ACKS	I	TVDD DVSS	Auto Setting Mode Select Pin in Pin Control mode “L”: Manual Setting mode, “H”: Auto Setting mode	Hi-Z
	CAD1	I		Chip Address 1 Pin in Register Control mode	
19	TDM0	I	TVDD DVSS	TDM Mode Select Pin in Pin Control mode	Hi-Z
	DCLK2	I		DSD Clock Input Pin in DSD mode (DSDPATH bit = “0”)	
20	TDM1	I	TVDD DVSS	TDM Mode Select Pin in Pin Control mode	Hi-Z
21	DCHAIN	I	TVDD DVSS	Daisy Chain mode Enable Pin in Pin Control mode	Hi-Z
22	INVR	I	TVDD DVSS	Rch Output Signal Invert Enable Pin in Pin Control mode	Hi-Z
23	TESTE	I	TVDD DVSS	Test mode Enable Pin (Internal pull-down pin)	Pull-down to DVSS (typ. 100 kΩ)
24 25 26	VREFHR	I	VDDR VSSR	Rch High Level Voltage Reference Input Pin	Hi-Z
27 28 29	VREFLR	I	VDDR VSSR	Rch Low Level Voltage Reference Input Pin	Connected to VCMR (typ. 5 kΩ)
30	VCMR	O	VDDR VSSR	Rch Common Voltage Pin, Normally connected to VREFLR with a 10 μF electrolytic cap. This pin is prohibited to connect to other devices.	Connected to VREFLR (typ. 5 kΩ)
31 32	AOUTRN	O	VDDR VSSR	Rch Negative Analog Output Pin	Connected to AOUTRP (typ. 300 kΩ)
33 34	AOUTRP	O	VDDR VSSR	Rch Positive Analog Output Pin	Connected to AOUTRN (typ. 300 kΩ)

No.	Pin Name	I/O	Protection Diode	Function	Power Down State
35 36 37	VDDR	-	-	Rch Analog Power Supply Pin	-
38 39 40	VSSR	-	-	Analog Ground Pin	-
41 42 43	VSSL	-	-	Analog Ground Pin	-
44 45 46	VDDL	-	-	Lch Analog Power Supply Pin	-
47 48	AOUTP	O	VDDL VSSL	Lch Positive Analog Output Pin	Connected to AOUTLN (typ. 300 kΩ)
49 50	AOUTLN	O	VDDL VSSL	Lch Negative Analog Output Pin	Connected to AOUTLP (typ. 300 kΩ)
51	VCML	O	VDDL VSSL	Lch Common Voltage Pin Normally connected to VREFLL with a 10 µF electrolytic cap. This pin is prohibited to connect to other devices.	Connected to VREFLL (typ. 5 kΩ)
52 53 54	VREFLL	I	VDDL VSSL	Lch Low Level Voltage Reference Input Pin	Connected to VCML (typ. 5 kΩ)
55 56 57	VREFHL	I	VDDL VSSL	Lch High Level Voltage Reference Input Pin	Hi-Z
58	EXTR	I	VDDL VSSL	External Resistor Connect Pin Connect 33 kΩ (±0.1%) to AVSS	Hi-Z
59	AVDD	-	-	(LDOE pin = "H") Analog Power Supply Pin, 3.0 to 3.6 V (LDOE pin = "L") Analog Power Supply Pin, DVDD to 3.6 V	-
60	AVSS	-	-	Analog Ground Pin	-
61	MCLK	I	AVDD AVSS	Master Clock Input Pin	Hi-Z
62	DVDD	O	-	(LDOE pin = "H") LDO Output Pin. This pin should be connected to DVSS with 1 µF (±50%). This pin is prohibited to connect to other devices.	Pull-down to DVSS (typ. 500 Ω)
		-		(LDOE pin = "L") Digital Power Supply Pin, 1.7 to 1.98 V	Hi-Z
63	DVSS	-	-	Digital Ground Pin	-
64	TVDD	-	-	(LDOE pin = "H") Digital Power Supply Pin, 3.0 to 3.6 V (LDOE pin = "L") Digital Power Supply Pin, DVDD to 3.6 V	-
Exposed Pad			-	Connect to AVSS	-

Note 1. All input pins except internal pull-up/down pins must not be left floating.
Note 2. The AK4497S must be reset by PDN pin after changing the control mode (Pin Control ⇔ Register Control) by the PSN pin.
Note 3. PCM mode, DSD mode and EXDF mode are controlled by register settings.

5.4. Handling of Unused Pin

Unused I/O pins must be connected appropriately.

5.4.1. Pin Control mode (PCM mode only)

Classification	Pin Name	Recommended setting
Analog	AOUTLP, AOUTLN	Open
	AOUTRP, AOUTRN	Open
	VCML, VCMR	Open
	VREFHL, VREFHR	Connect to VDDL, VDDR
	VREFLL, VREFLR	Connect to VSSL, VSSR
Digital	TESTE	Connect to DVSS
	TDMO	Open

5.4.2. Register Control mode

PCM mode

Classification	Pin Name	Recommended setting
Analog	AOUTLP, AOUTLN	Open
	AOUTRP, AOUTRN	Open
	VCML, VCMR	Open
	VREFHL, VREFHR	Connect to VDDL, VDDR
	VREFLL, VREFLR	Connect to VSSL, VSSR
Digital	SSLOW, DEM0, GAIN, TDM0, TDM1, DCHAIN, INVR, TESTE	Connect to DVSS
	CSN (In I^2C-bus Control mode)	Connect to DVSS
	TDMO, DZFL, DZFR	Open

DSD mode

DSDPATH bit = “0”

Classification	Pin Name	Recommended setting
Analog	AOUTLP, AOUTLN	Open
	AOUTRP, AOUTRN	Open
	VCML, VCMR	Open
	VREFHL, VREFHR	Connect to VDDL, VDDR
	VREFLL, VREFLR	Connect to VSSL, VSSR
Digital	BICK, SDATA, LRCK, WCK, TDM1, DCHAIN, INVR, TESTE	Connect to DVSS
	CSN (In I^2C-bus Control mode)	Connect to DVSS
	TDMO, DZFL, DZFR	Open

DSDPATH bit = “1”

Classification	Pin Name	Recommended setting
Analog	AOUTLP, AOUTLN	Open
	AOUTRP, AOUTRN	Open
	VCML, VCMR	Open
	VREFHL, VREFHR	Connect to VDDL, VDDR
	VREFLL, VREFLR	Connect to VSSL, VSSR
Digital	DEM0, GAIN, TDM0, WCK, TDM1, DCHAIN, INVR, TESTE	Connect to DVSS
	CSN (In I^2C-bus Control mode)	Connect to DVSS
	TDMO, DZFL, DZFR	Open

EXDF mode

Classification	Pin Name	Recommended setting
Analog	AOUTLP, AOUTLN	Open
	AOUTRP, AOUTRN	Open
	VCML, VCMR	Open
	VREFHL, VREFHR	Connect to VDDL, VDDR
	VREFLL, VREFLR	Connect to VSSL, VSSR
Digital	DEM0, GAIN, TDM0, TDM1, DCHAIN, INVR, TESTE	Connect to DVSS
	CSN (In I^2C-bus Control mode)	Connect to DVSS
	TDMO, DZFL, DZFR	Open

6. Absolute Maximum Ratings

(AVSS = DVSS = VSSL = VSSR = VREFLL = VREFLR = 0 V; Note 4, Note 5)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies:	Digital I/O	TVDD	−0.3	4.0	V
	Digital Core	DVDD	−0.3	2.35	V
	Clock Interface	AVDD	−0.3	4.0	V
	Analog	VDDL/R	−0.3	6.0	V
	|AVSS − DVSS|	ΔGND	-	0.3	V
	|AVSS − VSSL|	ΔGND	-	0.3	V
	|AVSS − VSSR|	ΔGND	-	0.3	V
	|DVSS − VSSL|	ΔGND	-	0.3	V
	|DVSS − VSSR|	ΔGND	-	0.3	V
	|VSSL − VSSR|	ΔGND	-	0.3	V
Voltage Reference	“H” Voltage Reference (Note 6)	VREFHL/R	−0.3	VDDL/R + 0.3 or 6.0	V
	“L” Voltage Reference	VREFLL/R	−0.3	+0.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Digital Input Voltage (Note 7)		VIND	−0.3	TVDD + 0.3 or 4.0	V
Ambient Temperature (Power supplied) (Note 5)		Ta	−40	105	°C
Storage Temperature		Tstg	−65	150	°C

Note 4. All voltages with respect to ground.

Note 5. AVSS, DVSS, VSSL and VSSR must be connected to the same analog ground plane. The exposed pad on the bottom of the package must be soldered to the analog ground plane on the printed circuit board.

Note 6. Regarding VREFHL/R pins, the maximum value is lower of (VDDL/R + 0.3 V) or 6.0 V.

Note 7. Regarding Digital input pins, the maximum value is lower of (TVDD + 0.3 V) or 4.0 V.
The maximum value for MCLK is lower of (AVDD + 0.3 V) or 4.0 V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(AVSS = DVSS = VSSL = VSSR = VREFLL = VREFLR = 0 V; Note 4, Note 5)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies (Note 9), (Note 10)	LDOE pin = "L"					
	Digital I/O	TVDD	DVDD	1.8	3.6	V
	Clock Interface	AVDD	DVDD	1.8	3.6	V
	Digital Core	DVDD	1.7	1.8	1.98	V
	Analog	VDDL/R	4.75	5.0	5.25	V
	LDOE pin = "H"					
	Digital I/O	TVDD	3.0	3.3	3.6	V
	Clock Interface	AVDD	3.0	3.3	3.6	V
	Analog	VDDL/R	4.75	5.0	5.25	V
Voltage Reference (Note 8)	"H" voltage reference	VREFHL/R	VDDL/R−0.5	-	VDDL/R	V
	"L" voltage reference	VREFLL/R	-	VSSL/R	-	V

Note 8. The analog output voltage scales with the voltage of (VREFHL/R − VREFLL/R).
Note 9. When not using the internal LDO (LDOE pin = "L"), TVDD must be powered up before DVDD or at the same time. Other than that, there are no restrictions on the order of power-up.
Note 10. The internal LDO outputs DVDD (typ. 1.8 V) when the LDOE pin = "H". Also, there are no restrictions on the order of power-up.

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

8. Electrical Characteristics

8.1. Analog Characteristics

8.1.1. PCM mode

(Ta = 25 °C; LDOE pin = “L”, AVDD = TVDD = 3.3 V, DVDD = 1.8 V, AVSS = DVSS = VSSL/R = 0 V; VREFHL/R = VDDL/R = 5.0 V, VREFLL/R = 0 V; Input data = 24-bit; BICK = 64fs; Signal Frequency = 1 kHz; Sampling Frequency = 44.1 kHz; Measurement bandwidth = 20 Hz – 20 kHz; External Circuit: Figure 85; SC[2:0] bit = “000”; ±2.8 Vpp output (GC[2:0] bits = “000” or GAIN pin = “L”); Heavy Load mode = off (HLOAD bit = “0” or HLOAD pin = “L”); unless otherwise specified.)

Parameter					Min.	Typ.	Max.	Unit
Resolution					-	-	32	Bits
Dynamic Characteristics (Note 11)								
THD+N	fs=44.1 kHz	BW = 20 kHz	0 dBFS	GC[2:0]= “000” or GAIN= “L”	-	−117	−108	dB
				GC[2:0]= “100” or GAIN= “H”	-	−113	-	
			−60 dBFS		-	−66	-	dB
	fs=96 kHz	BW = 40 kHz	0 dBFS		-	−114	-	dB
			−60 dBFS		-	−63	-	dB
	fs=192 kHz	BW = 40 kHz	0 dBFS		-	−114	-	
			−60 dBFS		-	−63	-	dB
		BW = 80 kHz	−60 dBFS		-	−60	-	dB
	fs=384 kHz	BW = 40 kHz	0 dBFS		-	-114	-	dB
	fs=768 kHz	BW = 40kHz	0 dBFS		-	-113	-	dB
Dynamic Range (−60 dBFS with A-weighted) (Note 12)					125	129	-	dB
S/N (A-weighted) (Note 13)	GC[2:0]= “000” or GAIN= “L”				125	129	-	dB
	GC[2:0]= “100” or GAIN= “H”			Stereo mode	-	131	-	dB
				Mono mode (Note 19)	-	133	-	
Interchannel Isolation (1 kHz)					110	120	-	dB
DC Accuracy								
Interchannel Gain Mismatch					-	0.1	0.3	dB
Gain Drift (Note 14)					-	20	-	ppm/°C
Output Voltage	GC[2:0] bits=“000” or GAIN pin=“L” (Note 15)				±2.65	±2.8	±2.95	Vpp
	GC[2:0] bits=“100” or GAIN pin=“H” (Note 16)				±3.55	±3.75	±3.95	Vpp
Load Resistance (Note 17)	HLOAD bit=“0” or HLOAD pin=“L”				8	10	-	kΩ
	HLOAD bit=“1” or HLOAD pin=“H”				120	-	-	Ω
Load Capacitance (Note 18)					-	-	25	pF

Note 11. Measured by Audio Precision APx555. Averaging mode.
Note 12. 101 dB (typ.) at 16-bit data and 118 dB (typ.) at 20-bit data.
Note 13. S/N does not depend on the input data bit length.
Note 14. The voltage on (VREFH − VREFL) is held +5 V externally.
Note 15. The analog output voltage with 0 dBFS input signal when GC[2:0] bits = “000” or the GAIN pin = “L” is calculated by the following formula.
AOUTL/R (typ.@ 0 dB) = (AOUTP) − (AOUTN) = ±2.8 Vpp × (VREFHL/R − VREFLL/R) / 5
Note 16. The analog output voltage with 0 dBFS input signal when GC[2:0] bits = “100” or the GAIN pin = “H” is calculated by the following formula.
AOUTL/R (typ.@ 0 dB) = (AOUTP) − (AOUTN) = ±3.75 Vpp × (VREFHL/R − VREFLL/R) / 5
Note 17. Regarding Load Resistance, AC load is 8k Ω (min.) with a DC cut capacitor when HLOAD bit = “0” or the HLOAD pin = “L”. DC load is 120 Ω (min.) without a DC cut capacitor if the HLOAD bit = “1” or HLOAD pin = “H”. The load resistance value is with respect to ground. Analog characteristics are sensitive to capacitive load that is connected to the output pin. Therefore, the capacitive load must be minimized.
Note 18. The load capacitance value is with respect to ground.

Note 19. This mode is shown in Figure 86.

(Ta = 25 °C; AVDD = TVDD = 3.3 V, DVDD = 1.8 V(@LDOE pin = “L”), AVSS = DVSS = VSSL/R = 0 V; VREFHL/R = VDDL/R = 5.0 V, VREFLL/R = 0 V; Input data = 24-bit; BICK = 64fs; Signal Frequency = 1 kHz; Sampling Frequency = 44.1 kHz; SC[2:0] bits = “000”); ±2.8 Vpp output mode (GC[2:0] bits = “000” or GAIN pin = “L”); Heavy Load mode = off (HLOAD bit = “0” or HLOAD pin = “L”); unless otherwise specified.)

Power Supplies					
Parameter		**Min.**	**Typ.**	**Max.**	**Unit**
Power Supply Current					
Normal operation (PDN pin = “H”, HLOAD bit = “0” or HLOAD pin = “L”)					
VDDL + VDDR		-	60	90	mA
VREFHL, VREFHR (each pin)		-	1	1.5	mA
AVDD		-	1	1.5	mA
TVDD					
LDOE pin = “H”	fs = 44.1 kHz	-	7	11	mA
	fs = 96 kHz	-	12	18	mA
	fs = 192 kHz	-	18	27	mA
LDOE pin = “L”		-	1	1.5	mA
DVDD					
LDOE pin = “L”	fs = 44.1 kHz	-	6	9	mA
	fs = 96 kHz	-	11	17	mA
	fs = 192 kHz	-	17	26	mA
Total Current per Channel LDOE pin = “H”, fs = 44.1 kHz, HLOAD pin = “H”		-	46	72	mA/ch
Power down (PDN pin = “L”) (Note 20)					
LDOE pin = “L”, TVDD = 1.8 V TVDD + AVDD + VDDL/R + VREFHL/R + DVDD		-	20	120	µA
LDOE pin = “H”, TVDD = 3.3 V (Note 21) TVDD + AVDD + VDDL/R + VREFHL/R		-	10	100	µA

Note 20. The PSN pin = TVDD, and all other digital input pins including clock pins (MCLK, BICK and LRCK) = DVSS.

Note 21. The DVDD pin becomes an output pin when the LDOE pin = “H”.

8.1.2. DSD mode

(Ta = 25 °C; AVDD = TVDD = 3.3 V, DVDD = 1.8 V (@LDOE pin = “L”), AVSS = DVSS = VSSL/R = 0 V; VREFHL/R = VDDL/R = 5.0 V, VREFLL/R = 0 V; Signal Frequency = 1 kHz; Measurement bandwidth = 20 Hz to 20 kHz; External Circuit; Example circuit 3 (Figure 85); SC[2:0] bit = “000”; ±2.8 Vpp output mode (GC[2:0] bits = “000” or GAIN pin = “L”); Heavy Load mode = off (HLOAD bit = “0” or HLOAD pin = “L”); unless otherwise specified.)

Parameter		Min.	Typ.	Max.	Unit
Dynamic Characteristics (Note 22)					
THD+N	0 dBFS	-	−114	-	dB
S/N (A-weighted, Normal path)	Digital “0” (Note 24)	-	129	-	dB
DC Accuracy (Note 23)					
Output Voltage (Normal path)	(Note 25)	±2.65	±2.8	±2.95	Vpp
Output Voltage (Volume Bypass)	(Note 26)	±2.38	±2.5	±2.63	Vpp

Note 22. This is measurement reference value with AKM evaluation board.
DSD Data stream: DSD64, DSD128, DSD256 Input signals are generated by AK4137.
DSD512 signal is AKM original.

Note 23. The output level is assumed as 0 dB when a 1 kHz 25 % to 75 % duty sine wave is input.
Click noise may occur if the input signal exceeds 0 dB.

Note 24. Digital “0” is a digital zero code pattern (“01101001”).

Note 25. When DSDD bit = “0” (Normal Path), the analog output voltage at 25 % to 75 % input signal duty is calculated by the following equation.
Output Voltage (typ. @ 0 dB) = (AOUTLP/RP) − (AOUTLN/RN)
= ±2.8 Vpp × (VREFHL/R − VREFLL/R) / 5.0

Note 26. When DSDD bit = “1” (Volume Bypass), the analog output voltage with 25 % to 75 % input signal duty is calculated by the following equation.
Output Voltage (typ. @ 0 dB) = (AOUTLP/RP) − (AOUTLN/RN)
= ±2.5 Vpp × (VREFHL/R − VREFLL/R) / 5.0.

8.2. Sharp Roll-Off Filter Characteristics

(Ta = −40 to 105 °C; VDDL/R = 4.75 to 5.25 V, AVDD = TVDD = 1.7 to 3.6 V, DVDD = 1.7 to 1.98 V; DEM = OFF; SD bit = “0” or SD pin = “L”, SLOW bit = “0” or SLOW pin = “L”, SSLOW bit = “0” or SSLOW pin = “L”)

8.2.1. Normal Speed mode (fs = 44.1 kHz)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 27)	±0.01 dB −6.0 dB	- -	0 -	- 22.05	20.0 -	kHz kHz
Passband	(Note 28)	PB	0	-	20.0	kHz
Stopband	(Note 28)	SB	24.1	-	-	kHz
Passband Ripple	(Note 29)	PR	-	-	±0.005	dB
Stopband Attenuation	(Note 27)	SA	100	-	-	dB
Group Delay	(Note 30)	GD	-	29.2	-	1/fs
Digital Filter + SCF	(Note 27)					
Frequency Response: 0 to 20.0 kHz		-	−0.2	-	+0.1	dB

8.2.2. Double Speed mode (fs = 96 kHz)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 27)	±0.01 dB −6.0 dB	- -	0 -	- 48.0	43.5 -	kHz kHz
Passband	(Note 28)	PB	0	-	43.5	kHz
Stopband	(Note 28)	SB	52.5	-	-	kHz
Passband Ripple	(Note 29)	PR	-	-	±0.005	dB
Stopband Attenuation	(Note 27)	SA	100	-	-	dB
Group Delay	(Note 30)	GD	-	29.2	-	1/fs
Digital Filter + SCF	(Note 27)					
Frequency Response: 0 to 40.0 kHz		-	−0.6	-	+0.1	dB

8.2.3. Quad Speed mode (fs = 192 kHz)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 27)	±0.01 dB −6.0 dB	- -	0 -	- 96.0	87.0 -	kHz kHz
Passband	(Note 28)	PB	0	-	87.0	kHz
Stopband	(Note 28)	SB	104.9	-		kHz
Passband Ripple	(Note 29)	PR	-	-	±0.005	dB
Stopband Attenuation	(Note 27)	SA	100	-	-	dB
Group Delay	(Note 30)	GD	-	29.2	-	1/fs
Digital Filter + SCF	(Note 27)					
Frequency Response: 0 to 80.0 kHz		-	−2.0	-	+0.1	dB

Note 27. Frequency response refers to the output level (0 dB) of a 1 kHz, 0 dB sine wave input. Stopband attenuation band ranges from SB to 4fs.
Note 28. The passband and stopband frequencies scale with fs. For example, PB = 0.4535 × fs (@ ±0.01 dB), SB = 0.546 × fs.
Note 29. This value is the gain amplitude of first step interpolator which is 4 times oversampling filter in pass band width.
Note 30. The calculating delay time which occurred by digital filtering. This time is from setting the 16/20/24/32-bit data of both channels to the output of analog signal.

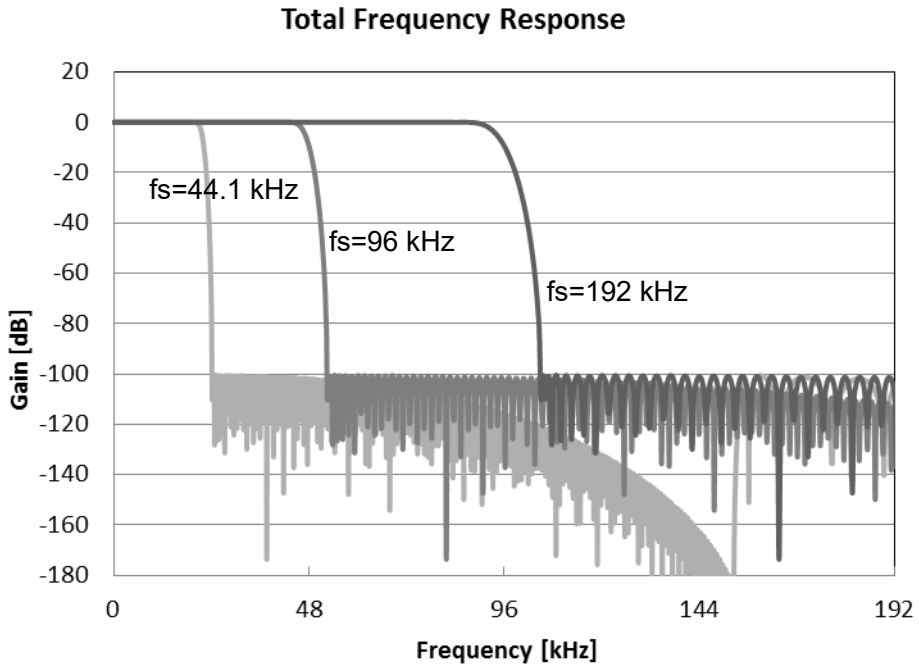


Figure 3. Sharp Roll-off Filter Frequency Response

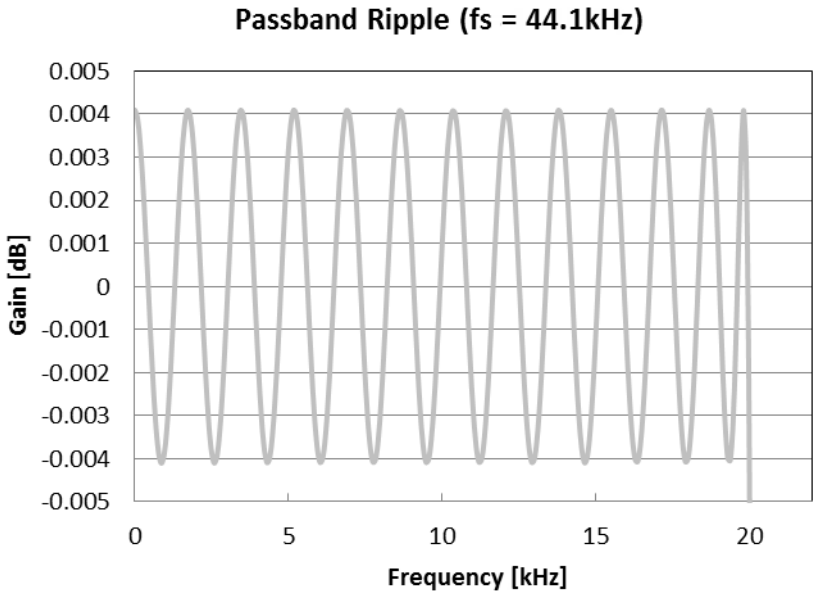


Figure 4. Sharp Roll-off Filter Passband Ripple

8.3. Slow Roll-Off Filter Characteristics

(Ta = −40 to 105 °C; VDDL/R = 4.75 to 5.25 V, AVDD = TVDD = 1.7 to 3.6 V, DVDD = 1.7 to 1.98 V; DEM = OFF; SD bit = “0” or SD pin = “L”, SLOW bit = “1” or SLOW pin = “H”, SSLOW bit = “0” or SSLOW pin = “L”)

8.3.1. Normal Speed mode (fs = 44.1 kHz)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 27)	±0.01 dB −6.0 dB	PB -	0 -	- 21.0	8.0 -	kHz kHz
Passband	(Note 31)	PB	0	-	8.0	kHz
Stopband	(Note 31)	SB	39.2	-	-	kHz
Passband Ripple	(Note 29)	PR	-	-	±0.007	dB
Stopband Attenuation	(Note 27)	SA	92	-	-	dB
Group Delay	(Note 30)	GD	-	6.5	-	1/fs
Digital Filter + SCF	(Note 27)					
Frequency Response: 0 to 20.0 kHz		-	−5.0	-	+0.1	dB

8.3.2. Double Speed mode (fs = 96 kHz)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 27)	±0.01 dB −6.0 dB	PB	0 -	- 45.6	17.6 -	kHz kHz
Passband	(Note 31)	PB	0	-	17.6	kHz
Stopband	(Note 31)	SB	85.4	-	-	kHz
Passband Ripple	(Note 29)	PR	-	-	±0.007	dB
Stopband Attenuation	(Note 27)	SA	92	-	-	dB
Group Delay	(Note 30)	GD	-	6.5	-	1/fs
Digital Filter + SCF	(Note 27)					
Frequency Response: 0 to 40.0 kHz		-	−3.8	-	+0.1	dB

8.3.3. Quad Speed mode (fs = 192 kHz)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 27)	±0.01 dB −6.0 dB	- -	0 -	- 91.2	35.2 -	kHz kHz
Passband	(Note 31)	PB	0	-	35.2	kHz
Stopband	(Note 31)	SB	170.7	-	-	kHz
Passband Ripple	(Note 29)	PR	-	-	±0.007	dB
Stopband Attenuation	(Note 27)	SA	100	-	-	dB
Group Delay	(Note 30)	GD	-	6.5	-	1/fs
Digital Filter + SCF	(Note 27)					
Frequency Response: 0 to 80.0 kHz		-	−5.0	-	+0.1	dB

Note 27. Frequency response refers to the output level (0 dB) of a 1 kHz, 0 dB sine wave input. Stopband attenuation band ranges from SB to 4fs.
Note 29. This value is the gain amplitude of first step interpolator which is 4 times oversampling filter in pass band width.
Note 30. The calculating delay time which occurred by digital filtering. This time is from setting the 16/20/24/32-bit data of both channels to the output of analog signal.
Note 31. The passband and stopband frequencies scale with fs. For example, PB = 0.1836 × fs (@±0.01 dB), SB = 0.8889 × fs.

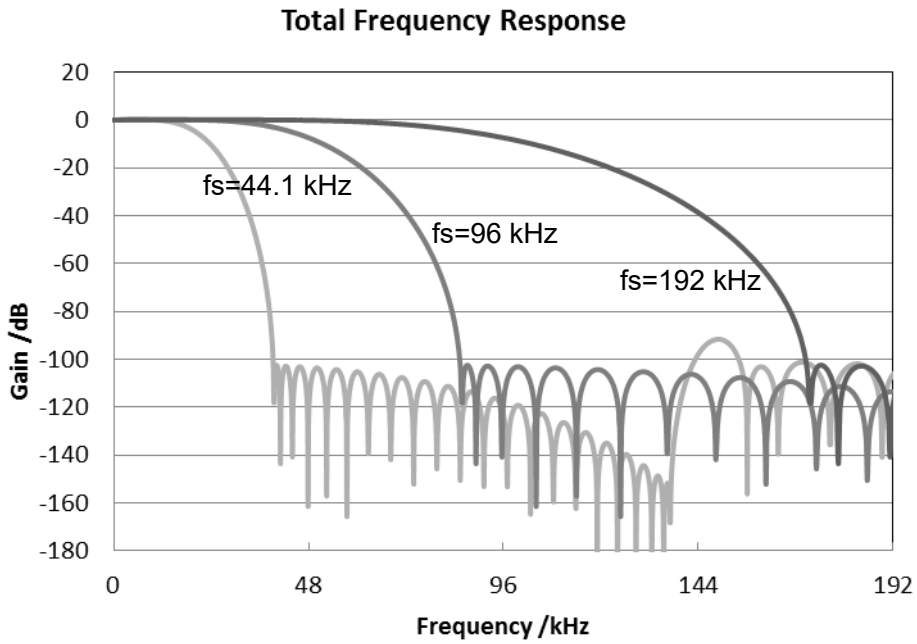


Figure 5. Slow Roll-off Filter Frequency Response

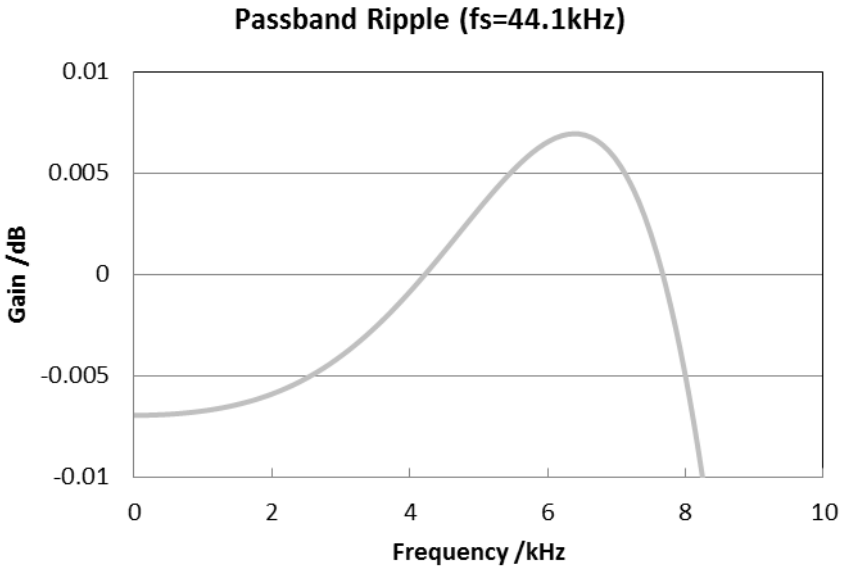


Figure 6. Slow Roll-off Filter Passband Ripple

8.4. Short Delay Sharp Roll-Off Filter Characteristics

(Ta = −40 to 105 °C; VDDL/R = 4.75 to 5.25 V, AVDD = TVDD =1.7 to 3.6 V, DVDD = 1.7 to 1.98 V; DEM = OFF; SD bit = “1” or SD pin = “H”, SLOW bit = “0” or SLOW bit = “L”, SSLOW bit = “0” or SSLOW pin = “L”)

8.4.1. Normal Speed mode (fs = 44.1 kHz)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 27)	±0.01 dB −6.0 dB	- -	0 -	- 22.05	20.0 -	kHz kHz
Passband	(Note 32)	PB	0	-	20.0	kHz
Stopband	(Note 32)	SB	24.1	-	-	kHz
Passband Ripple	(Note 29)	PR	-	-	±0.005	dB
Stopband Attenuation	(Note 27)	SA	100	-	-	dB
Group Delay	(Note 30)	GD	-	6.0	-	1/fs
Digital Filter + SCF	(Note 27)					
Frequency Response: 0 to 20.0 kHz		-	−0.2	-	+0.1	dB

8.4.2. Double Speed mode (fs = 96 kHz)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 27)	±0.01 dB −6.0 dB	- -	0 -	- 48.0	43.5 -	kHz kHz
Passband	(Note 32)	PB	0	-	43.5	kHz
Stopband	(Note 32)	SB	52.5	-	-	kHz
Passband Ripple	(Note 29)	PR	-	-	±0.005	dB
Stopband Attenuation	(Note 27)	SA	100	-	-	dB
Group Delay	(Note 30)	GD	-	6.0	-	1/fs
Digital Filter + SCF	(Note 27)					
Frequency Response: 0 to 40.0 kHz		-	−0.6	-	+0.1	dB

8.4.3. Quad Speed mode (fs = 192 kHz)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 27)	±0.01 dB −6.0 dB	- -	0 -	- 96.0	87.0 -	kHz kHz
Passband	(Note 32)	PB	0	-	87.0	kHz
Stopband	(Note 32)	SB	104.9	-	-	kHz
Passband Ripple	(Note 29)	PR	-	-	±0.005	dB
Stopband Attenuation	(Note 27)	SA	100	-	-	dB
Group Delay	(Note 30)	GD	-	6.0	-	1/fs
Digital Filter + SCF	(Note 27)					
Frequency Response: 0 to 80.0 kHz			−2.0	-	+0.1	dB

Note 27. Frequency response refers to the output level (0 dB) of a 1 kHz, 0 dB sine wave input. Stopband attenuation band ranges from SB to 4fs.
Note 29. This value is the gain amplitude of first step interpolator which is 4 times oversampling filter in pass band width.
Note 30. The calculating delay time which occurred by digital filtering. This time is from setting the 16/20/24/32-bit data of both channels to the output of analog signal.
Note 32. The passband and stopband frequencies scale with fs. For example, PB = 0.4535 × fs (@±0.01 dB), SB = 0.546 × fs.

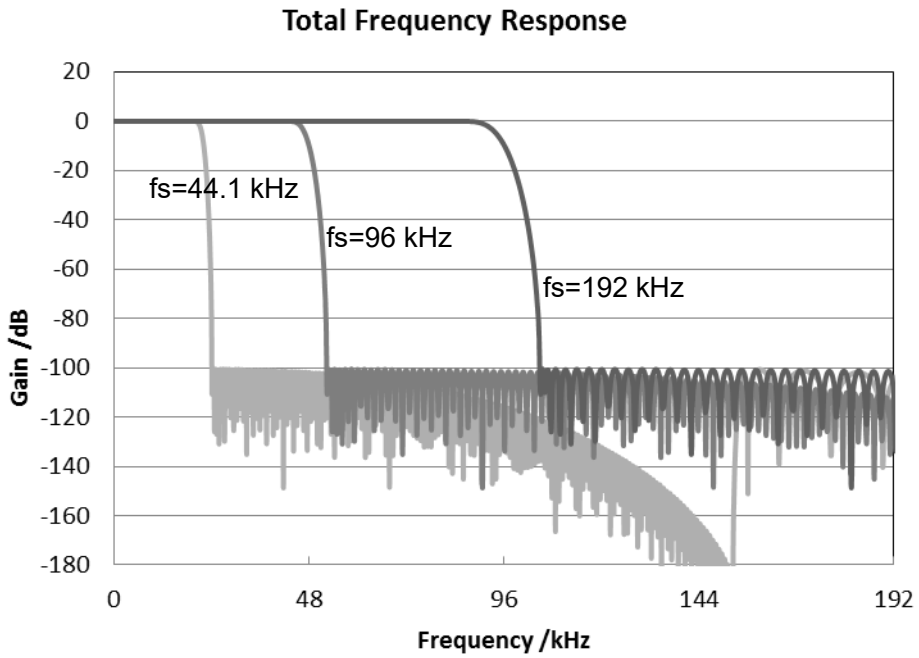


Figure 7. Short delay Sharp Roll-off Filter Frequency Response

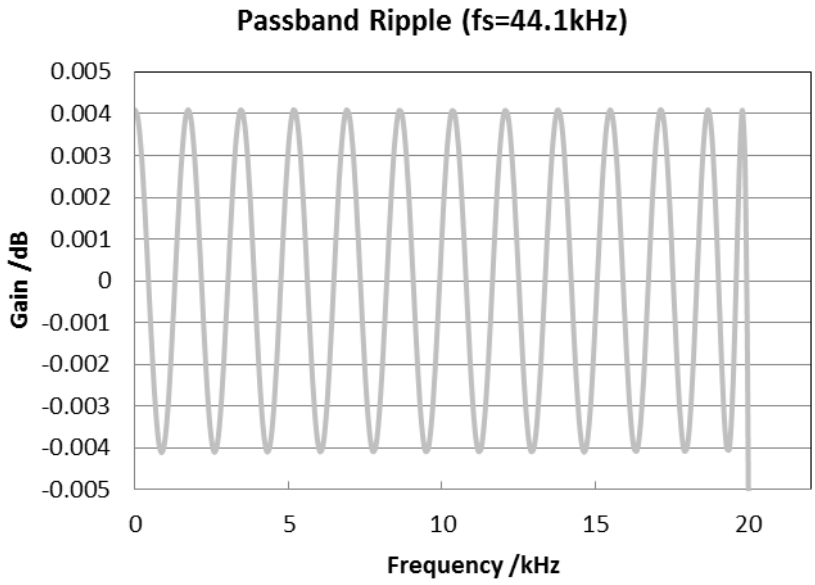


Figure 8. Short delay Sharp Roll-off Filter Passband Ripple

8.5. Short Delay Slow Roll-Off Filter Characteristics

(Ta = −40 to 105°C; VDDL/R = 4.75 to 5.25 V, AVDD = TVDD = 1.7 to 3.6 V, DVDD = 1.7 to 1.98 V; DEM = OFF; SD bit =“1” or SD pin = “H”, SLOW bit = “1” or SLOW pin = “H”, SSLOW bit = “0” or SSLOW pin =“L”)

8.5.1. Normal Speed mode (fs = 44.1 kHz)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 27)	±0.01 dB −6.0 dB	- -	0 -	- 21.0	8.0 -	kHz kHz
Passband	(Note 33)	PB	0	-	8.0	kHz
Stopband	(Note 33)	SB	39.2	-	-	kHz
Passband Ripple	(Note 29)	PR	-	-	±0.007	dB
Stopband Attenuation	(Note 27)	SA	92		-	dB
Group Delay	(Note 30)	GD	-	5.0	-	1/fs
Digital Filter + SCF	(Note 27)					
Frequency Response: 0 to 20.0 kHz		-	−5.0	-	+0.1	dB

8.5.2. Double Speed mode (fs = 96 kHz)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 27)	±0.01 dB −6.0 dB	- -	0 -	- 45.6	17.6 -	kHz kHz
Passband	(Note 33)	PB	0	-	17.6	kHz
Stopband	(Note 33)	SB	85.4	-	-	kHz
Passband Ripple	(Note 29)	PR	-	-	±0.005	dB
Stopband Attenuation	(Note 27)	SA	100	-	-	dB
Group Delay	(Note 30)	GD	-	5.0	-	1/fs
Digital Filter + SCF	(Note 27)					
Frequency Response: 0 to 40.0 kHz		-	−3.8	-	+0.1	dB

8.5.3. Quad Speed mode (fs = 192 kHz)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 27)	±0.01 dB −6.0 dB	- -	0 -	- 91.2	35.2 -	kHz kHz
Passband	(Note 33)	PB	0	-	35.2	kHz
Stopband	(Note 33)	SB	170.7	-	-	kHz
Passband Ripple	(Note 29)	PR	-	-	±0.005	dB
Stopband Attenuation	(Note 27)	SA	100	-	-	dB
Group Delay	(Note 30)	GD	-	5.0	-	1/fs
Digital Filter + SCF	(Note 27)					
Frequency Response: 0 to 80.0 kHz		-	−5.0	-	+0.1	dB

Note 27. Frequency response refers to the output level (0 dB) of a 1 kHz, 0 dB sine wave input. Stopband attenuation band ranges from SB to 4fs.
Note 29. This value is the gain amplitude of first step interpolator which is 4 times oversampling filter in pass band width.
Note 30. The calculating delay time which occurred by digital filtering. This time is from setting the 16/20/24/32-bit data of both channels to the output of analog signal.
Note 33. The passband and stopband frequencies scale with fs. For example, PB = 0.1836 × fs (@±0.01 dB), SB = 0.8866 × fs.

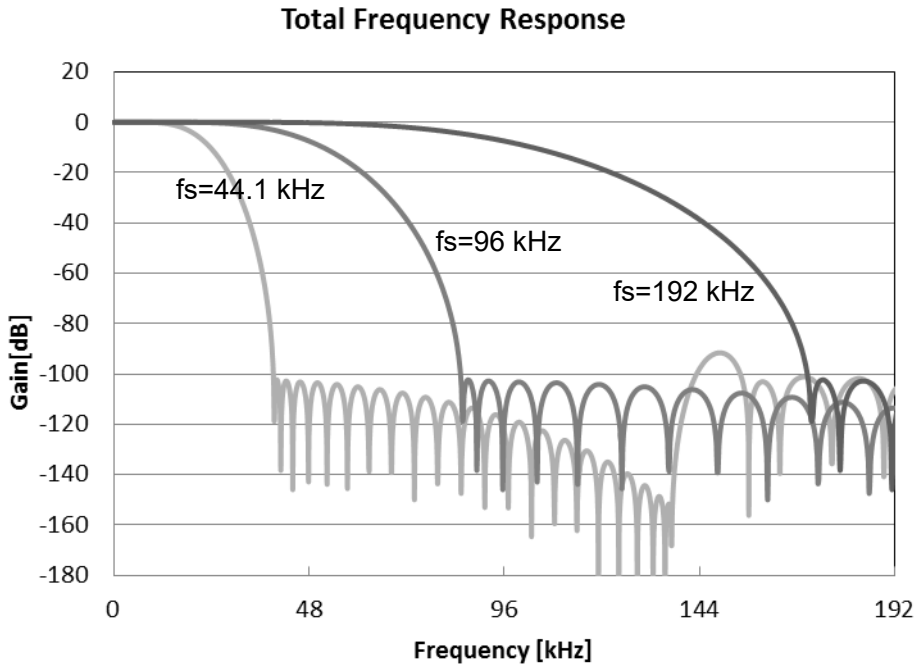


Figure 9. Short Delay Slow Roll-off Filter Frequency Response

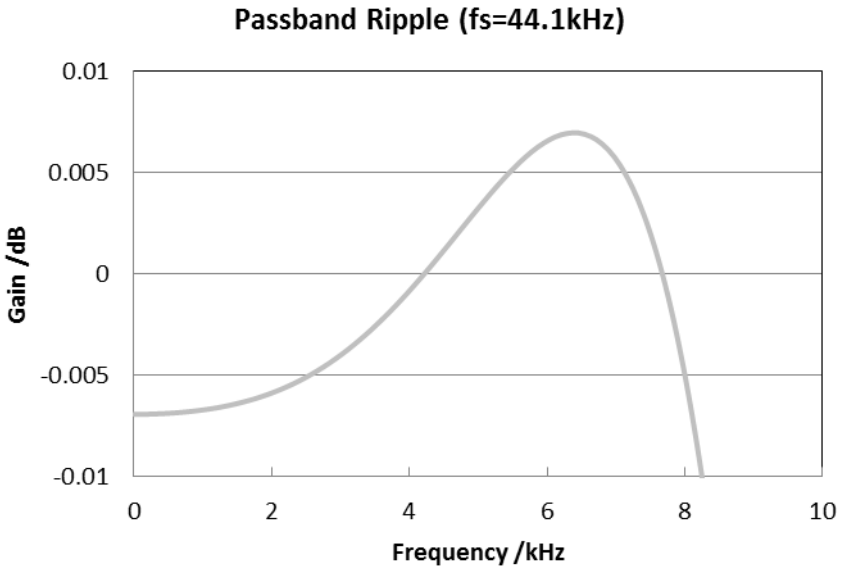


Figure 10. Short Delay Slow Roll-off Filter Passband Ripple

8.6. Low-Dispersion Short Delay Filter Characteristics

(Ta = −40 to 105 °C; VDDL/R = 4.75 to 5.25 V, AVDD = TVDD = 1.7 to 3.6 V, DVDD = 1.7 to 1.98 V; DEM = OFF; SD bit = “1” or SD pin = “H”, SLOW bit = “0” or SLOW pin = “L”, SSLOW bit = “1” or SSLOW pin = “H”)

8.6.1. Normal Speed mode (fs = 44.1 kHz)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 27)	±0.05 dB −6.0 dB	PB -	0 -	- 22.5	18.4 -	kHz kHz
Passband	(Note 34)	PB	0	-	18.4	kHz
Stopband	(Note 34)	SB	25.7	-	-	kHz
Passband Ripple	(Note 29)	PR	-	-	±0.05	dB
Stopband Attenuation	(Note 27)	SA	80	-	-	dB
Group Delay	(Note 29)	GD	-	10.0	-	1/fs
Group Delay Distortion		Δ GD	-	±0.035	-	1/fs
Digital Filter + SCF	(Note 27)					
Frequency Response: 0 to 20.0 kHz		-	−0.8	-	+0.1	dB

8.6.2. Double Speed mode (fs = 96 kHz)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 27)	±0.05 dB −6.0 dB	PB	0 -	- 48.0	40.1 -	kHz kHz
Passband	(Note 34)	PB	0	-	40.1	kHz
Stopband	(Note 34)	SB	55.9	-	-	kHz
Passband Ripple	(Note 29)	PR	-	-	±0.05	dB
Stopband Attenuation	(Note 27)	SA	80	-	-	dB
Group Delay	(Note 29)	GD	-	10.0	-	1/fs
Group Delay Distortion		Δ GD		±0.035	-	1/fs
Digital Filter + SCF	(Note 27)					
Frequency Response: 0 to 40.0 kHz			−0.6	-	+0.1	dB

8.6.3. Quad Speed mode (fs = 192 kHz)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Frequency Response (Note 27)	±0.05 dB −6.0 dB	- -	0 -	- 98.0	80.2 -	kHz kHz
Passband	(Note 34)	PB	0	-	80.2	kHz
Stopband	(Note 34)	SB	111.8	-	-	kHz
Passband Ripple	(Note 29)	PR	-	-	±0.05	dB
Stopband Attenuation	(Note 27)	SA	80	-	-	dB
Group Delay	(Note 29)	GD	-	10.0	-	1/fs
Group Delay Distortion		Δ GD	-	±0.035	-	1/fs
Digital Filter + SCF	(Note 27)					
Frequency Response: 0 to 80.0 kHz			−2.0	-	+0.1	dB

Note 27. Frequency response refers to the output level (0 dB) of a 1 kHz, 0 dB sine wave input. Stopband attenuation band ranges from SB to 4fs.

Note 29. This value is the gain amplitude of first step interpolator which is 4 times oversampling filter in pass band width.

Note 30. The calculating delay time which occurred by digital filtering. This time is from setting the 16/20/24/32-bit data of both channels to the output of analog signal.
Note 34. The passband and stopband frequencies scale with fs. For example, PB = 0.418 × fs (@±0.05dB), SB = 0.582 × fs.

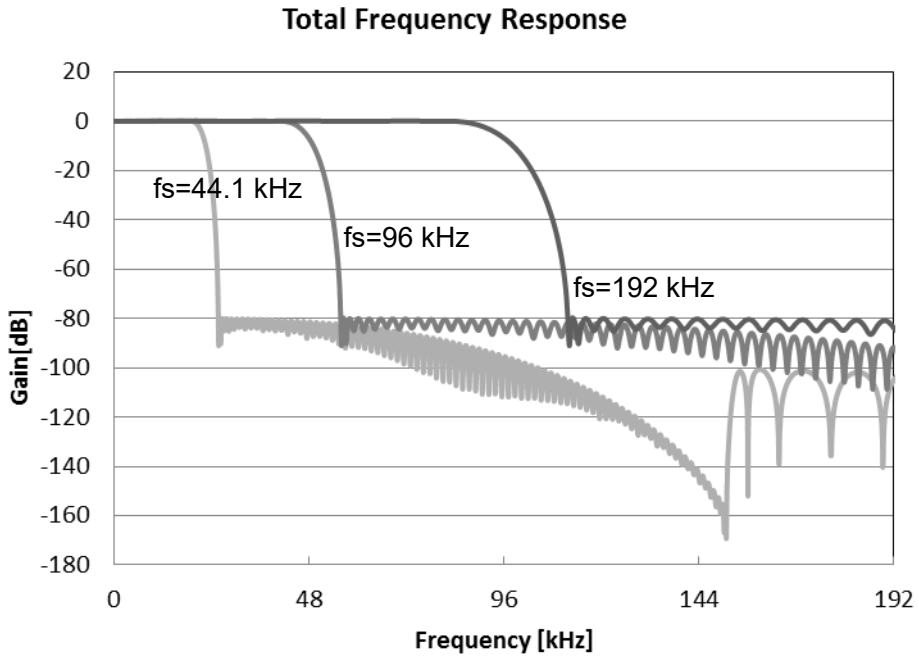


Figure 11. Low Dispersion Short Delay Filter Frequency Response

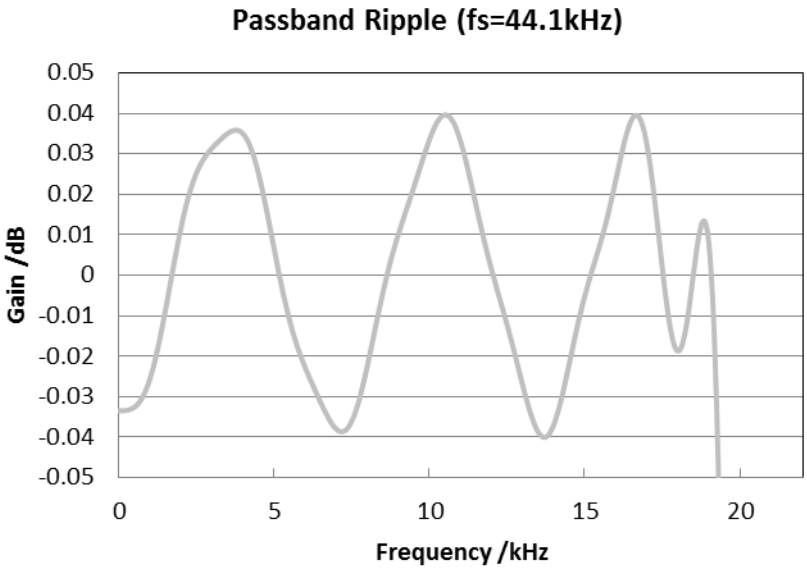


Figure 12. Low Dispersion Short Delay Filter Passband Ripple

8.7. DSD Filter Characteristics

(Ta = −40 to 105 °C; VDDL/R = 4.75 to 5.25 V, AVDD = TVDD = 1.7 to 3.6 V, DVDD = 1.7 to 1.98 V; fsb = 44.1kHz; DP bit = “1”, DSDF bit = “0”, DSDSEL[1:0] bits = “00”)

Parameter		Min.	Typ.	Max.	Unit
Digital Filter Response (Note 35)					
Frequency Response (Note 36)	20 kHz	-	−0.77	-	dB
	50 kHz	-	−5.25	-	dB
	100 kHz	-	−18.80	-	dB

(Ta = −40 to 105 °C; VDDL/R = 4.75 to 5.25 V, AVDD = TVDD = 1.7 to 3.6 V, DVDD = 1.7 to 1.98 V; fsb = 44.1 kHz; DP bit = “1”, DSDF bit = “1”, DSDSEL[1:0] bits = “00”)

Parameter		Min.	Typ.	Max.	Unit
Digital Filter Response (Note 35)					
Frequency Response (Note 36)	20 kHz	-	−0.19	-	dB
	100 kHz	-	−5.29	-	dB
	150 kHz	-	−15.57	-	dB

Note 35. The frequency response refers to the output level of 0 dB when a 1 kHz 25 % to 75 % duty sine wave is input.

Note 36. The frequency (20 k, 50 k, 100 k and 150 kHz) will be doubled when the sampling frequency is 128fsb (DSDSEL[1:0] bits = “01”) and it will be quadrupled when the sampling frequency is 256fsb (DSDSEL[1:0] bits = “10”).

8.8. DC Characteristics

(Ta = −40 to 105 °C; VDDL/R = 4.75 to 5.25 V, AVDD = TVDD = 1.7 to 3.6 V, DVDD = 1.7 to 1.98 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
MCLK					
1.7 ≦ AVDD ≦ 3.0 V			-		
High-Level Input Voltage	VIH1	80%AVDD	-	-	V
Low-Level Input Voltage	VIL1	-		20%AVDD	V
3.0 < AVDD ≦ 3.6 V					
High-Level Input Voltage	VIH1	70%AVDD	-		V
Low-Level Input Voltage	VIL1	-	-	30%AVDD	V
SDA, SCL					
1.7 ≦ TVDD ≦ 3.6 V			-		
High-Level Input Voltage	VIH3	70%TVDD	-	-	V
Low-Level Input Voltage	VIL3	-		30%TVDD	V
Digital input except MCLK, SDA and SCL					
1.7 ≦ TVDD ≦ 3.0 V			-		
High-Level Input Voltage	VIH2	80%TVDD	-	-	V
Low-Level Input Voltage	VIL2	-		20%TVDD	V
3.0 < TVDD ≦ 3.6 V					
High-Level Input Voltage	VIH2	70%TVDD	-		V
Low-Level Input Voltage	VIL2	-	-	30%TVDD	V
High-Level Output Voltage					
TDMO, DZFL, DZFR pins (Iout = −100 μA)	VOH	TVDD−0.3	-	-	V
Low-Level Output Voltage					
TDMO, DZFL, DZFR pins (Iout = 100 μA)	VOL	-	-	0.3	V
SDA pin (Iout = 3 mA, 2.0 V ≤ TVDD ≤ 3.6 V)	VOL	-	-	0.4	V
SDA pin (Iout = 3 mA, 1.7 V ≤ TVDD ≤ 2.0 V)	VOL	-	-	20%TVDD	V
Input Leakage Current (Note 37)	Iin	-	-	±10	μA

Note 37. The TESTE, TDMO, DIF0 and DIF1 pins have internal pull-down and the PSN pin has internal pull-up. Therefore, the TESTE, TDMO, DIF0, DIF1 and PSN pins are not included in this specification.

8.9. Switching Characteristics

(Ta = −40 to 105 °C; VDDL/R = 4.75 to 5.25 V, AVDD = TVDD = 1.7 to 3.6 V, DVDD = 1.7 to 1.98 V, C_L = 20 pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Master Clock Timing (Note 38)					
Frequency	fCLK	6.208	-	49.664	MHz
Duty Cycle	dCLK	40	-	60	%
High Pulse Width	tCLKH	9.05	-	-	ns
Low Pulse Width	tCLKL	9.05	-	-	ns
LRCK Clock Timing					
Normal mode (TDM[1:0] bits = "00")					
Frequency (fs)					
Normal Speed mode	fsn	30	-	54	kHz
Double Speed mode	fsd	54	-	108	kHz
Quad Speed mode	fsq	108	-	216	kHz
Oct speed mode	fso	216	-	388	kHz
Hex speed mode	fsh	388	-	776	kHz
Duty Cycle	Duty	45	-	55	%
TDM128 mode (TDM[1:0] bits = "01")					
Frequency (fs)					
Normal Speed mode	fsn	30	-	54	kHz
Double Speed mode	fsd	54	-	108	kHz
Quad Speed mode	fsq	108	-	216	kHz
High time	tLRH	1/128fs	-	-	ns
Low time	tLRL	1/128fs	-	-	ns
TDM256 mode (TDM[1:0] bits = "10")					
Frequency (fs)					
Normal Speed mode	fsn	30	-	54	kHz
Double Speed mode (Note 39)	fsd	54	-	108	kHz
High time	tLRH	1/256fs	-	-	ns
Low time	tLRL	1/256fs	-	-	ns
TDM512 mode (TDM[1:0] bits = "11")					
Frequency (fs)					
Normal Speed Mode (Note 40)	fsn	30	-	54	kHz
High time	tLRH	1/512fs	-	-	ns
Low time	tLRL	1/512fs	-	-	ns

Note 38. The MCLK frequency must be changed while the AK4497S is in reset state by setting the PDN pin = "L" or RSTN bit = "0".
Note 39. In Daisy Chain mode, fsd (max.) = 96 kHz if "TVDD < 3.0 V".
Note 40. In Daisy Chain mode, fsn (max.) = 48 kHz if "TVDD < 3.0 V".

(Ta = −40 to 105 °C; VDDL/R = 4.75 to 5.25 V, AVDD = TVDD = 1.7 to 3.6 V, DVDD = 1.7 to 1.98 V, C_L = 20 pF, PSN pin = “L”, AFSD bit = “1”)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Master Clock Timing (fs Auto Detect mode)					
Frequency	fCLK	6.208	-	49.664	MHz
Duty Cycle	dCLK	40	-	60	%
High Pulse Width	tCLKH	9.05	-	-	ns
Low Pulse Width	tCLKL	9.05	-	-	ns
LRCK Clock Timing (fs Auto Detect mode) (Note 41)					
Normal mode (TDM[1:0] bits = “00”)					
Frequency (fs)					
Normal Speed mode	fsn	30	-	54	kHz
Double Speed mode	fsd	87	-	108	kHz
Quad Speed mode	fsq	174	-	216	kHz
Oct speed mode	fso	360	-	388	kHz
Hex speed mode	fsh	696	-	776	kHz
Duty Cycle	Duty	45	-	55	%
TDM128 mode (TDM[1:0] bits = “01”)					
Frequency (fs)					
Normal Speed mode	fsn	30	-	54	kHz
Double Speed mode	fsd	87	-	108	kHz
Quad Speed mode	fsq	174	-	216	kHz
High time	tLRH	1/128fs	-	-	ns
Low time	tLRL	1/128fs	-	-	ns
TDM256 mode (TDM[1:0] bits = “10”)					
Frequency (fs)					
Normal Speed mode	fsn	30	-	54	kHz
Double Speed mode (Note 39)	fsd	87	-	108	kHz
High time	tLRH	1/256fs	-	-	ns
Low time	tLRL	1/256fs	-	-	ns
TDM512 mode (TDM[1:0] bits = “11”)					
Frequency (fs)					
Normal Speed mode (Note 40)	fsn	30	-	54	kHz
High time	tLRH	1/512fs	-	-	ns
Low time	tLRL	1/512fs	-	-	ns

Note 39. In Daisy Chain mode, fsd (max.) = 96 kHz if “TVDD < 3.0 V”.
Note 40. In Daisy Chain mode, fsn (max.) = 48 kHz if “TVDD < 3.0 V”.
Note 41. Normal operation is not guaranteed if a frequency not shown above is input to the LRCK.

Parameter		Symbol	Min.	Typ.	Max.	Unit
PCM Audio Serial Data Interface Timing						
Normal mode (TDM[1:0] bits = "00")						
BICK Period						
Normal Speed mode		tBCK	1/256fsn	-	-	ns
Double Speed mode		tBCK	1/128fsd	-	-	ns
Quad Speed mode		tBCK	1/64fsq	-	-	ns
Oct speed mode		tBCK	1/64fso	-	-	ns
Hex speed mode		tBCK	1/64fsh	-	-	ns
BICK Pulse Width Low		tBCKL	9	-	-	ns
BICK Pulse Width High		tBCKH	9	-	-	ns
BICK "↑" to LRCK Edge	(Note 42)	tBLR	5	-	-	ns
LRCK Edge to BICK "↑"	(Note 42)	tLRB	5	-	-	ns
SDATA Hold Time		tSDH	5	-	-	ns
SDATA Setup Time		tSDS	5	-	-	ns
TDM128 mode (TDM[1:0] bits = "01")						
BICK Period						
Normal Speed mode		tBCK	1/128fsn	-	-	ns
Double Speed mode		tBCK	1/128fsd	-	-	ns
Quad Speed mode		tBCK	1/128fsq	-	-	ns
BICK Pulse Width Low		tBCKL	14	-	-	ns
BICK Pulse Width High		tBCKH	14	-	-	ns
BICK "↑" to LRCK Edge	(Note 42)	tBLR	14	-	-	ns
LRCK Edge to BICK "↑"	(Note 42)	tLRB	14	-	-	ns
SDATA Hold Time		tSDH	5	-	-	ns
SDATA Setup Time		tSDS	5	-	-	ns
TDM256 mode (TDM[1:0] bits = "10")						
BICK Period						
Normal Speed mode		tBCK	1/256fsn	-	-	ns
Double Speed mode		tBCK	1/256fsd	-	-	ns
BICK Pulse Width Low		tBCKL	14	-	-	ns
BICK Pulse Width High		tBCKH	14	-	-	ns
BICK "↑" to LRCK Edge	(Note 42)	tBLR	14	-	-	ns
LRCK Edge to BICK "↑"	(Note 42)	tLRB	14	-	-	ns
TDMO Setup time BICK "↑"		tBSS	5	-	-	ns
TDMO Hold time BICK "↑"	(Note 43)	tBSH	5	-	-	ns
SDATA Hold Time		tSDH	5	-	-	ns
SDATA Setup Time		tSDS	5	-	-	ns
TDM512 mode (TDM[1:0] bits = "11")						
BICK Period						
Normal Speed mode		tBCK	1/512fsn	-	-	ns
BICK Pulse Width Low		tBCKL	14	-	-	ns
BICK Pulse Width High		tBCKH	14	-	-	ns
BICK "↑" to LRCK Edge	(Note 42)	tBLR	14	-	-	ns
LRCK Edge to BICK "↑"	(Note 42)	tLRB	14	-	-	ns
TDMO Setup time BICK "↑"		tBSS	5	-	-	ns
TDMO Hold time BICK "↑"	(Note 43)	tBSH	5	-	-	ns
SDATA Hold Time		tSDH	5	-	-	ns
SDATA Setup Time		tSDS	5	-	-	ns

Note 42. BICK rising edge must not occur at the same time as LRCK edge.
Note 43. LDOE pin = "L", tBSH (min.) = 4 ns if "TVDD > 2.6 V".

Parameter	Symbol	Min.	Typ.	Max.	Unit
PCM Audio Serial Data Interface Timing					
Base Sampling Frequency	fsb	30		192	kHz
External Digital Filter mode					
BCK Period	tB	27	-	-	ns
BCK Pulse Width Low	tBL	10	-	-	ns
BCK Pulse Width High	tBH	10	-	-	ns
BCK "↑" to WCK Edge	tBW	5	-	-	ns
WCK Period	tWCK	1.3	-	-	µs
WCK Edge to BCK "↑"	tWB	5	-	-	ns
WCK Pulse Width Low	tWCKL	54	-	-	ns
WCK Pulse Width High	tWCKH	54	-	-	ns
DINL/R Hold Time	tDH	5	-	-	ns
DINL/R Setup Time	tDS	5	-	-	ns
DSD Audio Serial Data Interface Timing					
Base Sampling Frequency	fsb	30		48	kHz
(DSD64 mode, DSDSEL[1:0] bits = "00")					
DCLK Period	tDCK	-	1/64fsb	-	ns
DCLK Pulse Width Low	tDCKL	144	-	-	ns
DCLK Pulse Width High	tDCKH	144	-	-	ns
DCLK Edge to DSDL/R (Note 44)	tDDD	–20	-	20	ns
(DSD128 mode, DSDSEL[1:0] bits = "01")					
DCLK Period	tDCK	-	1/128fsb	-	ns
DCLK Pulse Width Low	tDCKL	72	-	-	ns
DCLK Pulse Width High	tDCKH	72	-	-	ns
DCLK Edge to DSDL/R (Note 44)	tDDD	–10	-	10	ns
(DSD256 mode, DSDSEL[1:0] bits = "10")					
DCLK Period	tDCK	-	1/256fsb	-	ns
DCLK Pulse Width Low	tDCKL	36	-	-	ns
DCLK Pulse Width High	tDCKH	36	-	-	ns
DCLK Edge to DSDL/R (Note 44)	tDDD	–5	-	5	ns
(DSD512 mode, DSDSEL[1:0] bit = "11")					
DCLK Period	tDCK	-	1/512fsb	-	ns
DCLK Pulse Width Low	tDCKL	18	-	-	ns
DCLK Pulse Width High	tDCKH	18	-	-	ns
DSDL/R Setup Time	tDDS	5	-	-	ns
DSDL/R Hold Time	tDDH	5	-	-	ns

Note 44. DSD data transmitting device must meet this time. "tDDD" is defined from DCLK "↓" until DSDL/R edge when DCKB bit = "0" (default), "tDDD" is defined from DCLK "↑" until DSDL/R edge when DCKB bit = "1". If the audio serial data format is in Phase Modulation mode, "tDDD" is defined from DCLK edge "↓" or "↑" until DSDL/R edge regardless of DCKB bit setting.

Note 45. The AK4497S does not support Phase Modulation mode in DSD512 mode.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Control Interface Timing (3-wire Serial mode):					
CCLK Period	tCCK	200	-	-	ns
CCLK Pulse Width Low	tCCKL	80	-	-	ns
CCLK Pulse Width High	tCCKH	80	-	-	ns
CDTI Setup Time	tCDS	40	-	-	ns
CDTI Hold Time	tCDH	40	-	-	ns
CSN "H" Time	tCSW	150	-	-	ns
CSN "↓" to CCLK "↑"	tCSS	50	-	-	ns
CCLK "↑" to CSN "↑"	tCSH	50	-	-	ns
Control Interface Timing (I^2C-bus mode):					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling (Note 46)	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns
Capacitive load on bus	Cb	-	-	400	pF
Power down & Reset Timing (Note 47)					
PDN Accept Pulse Width	tAPD	600	-	-	ns
PDN Reject Pulse Width	tRPD	-	-	30	ns

Note 46. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.
Note 47. The AK4497S should be reset by bringing the PDN pin "L" upon power up.

8.10. Timing Diagram

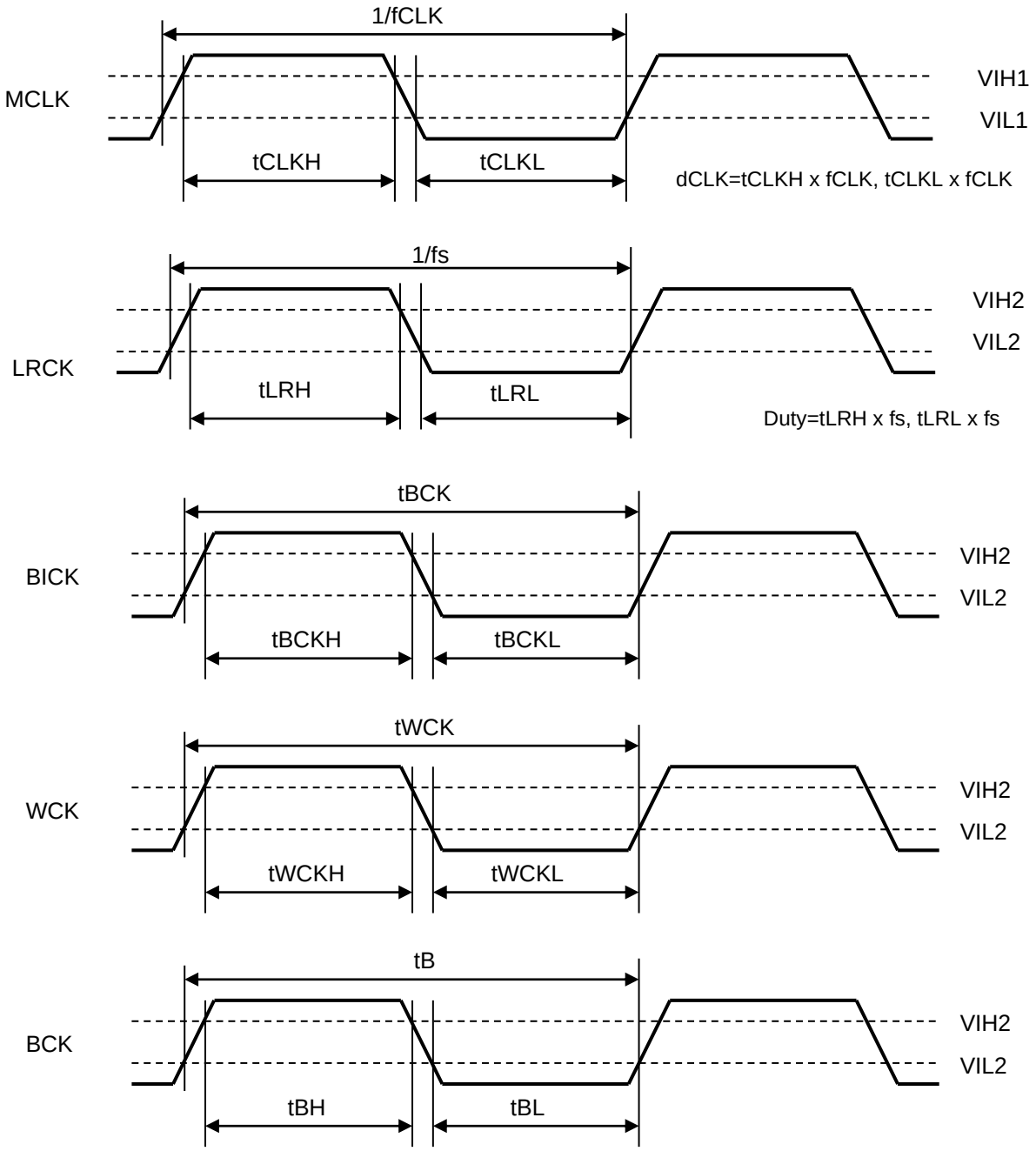


Figure 13. Clock Timing

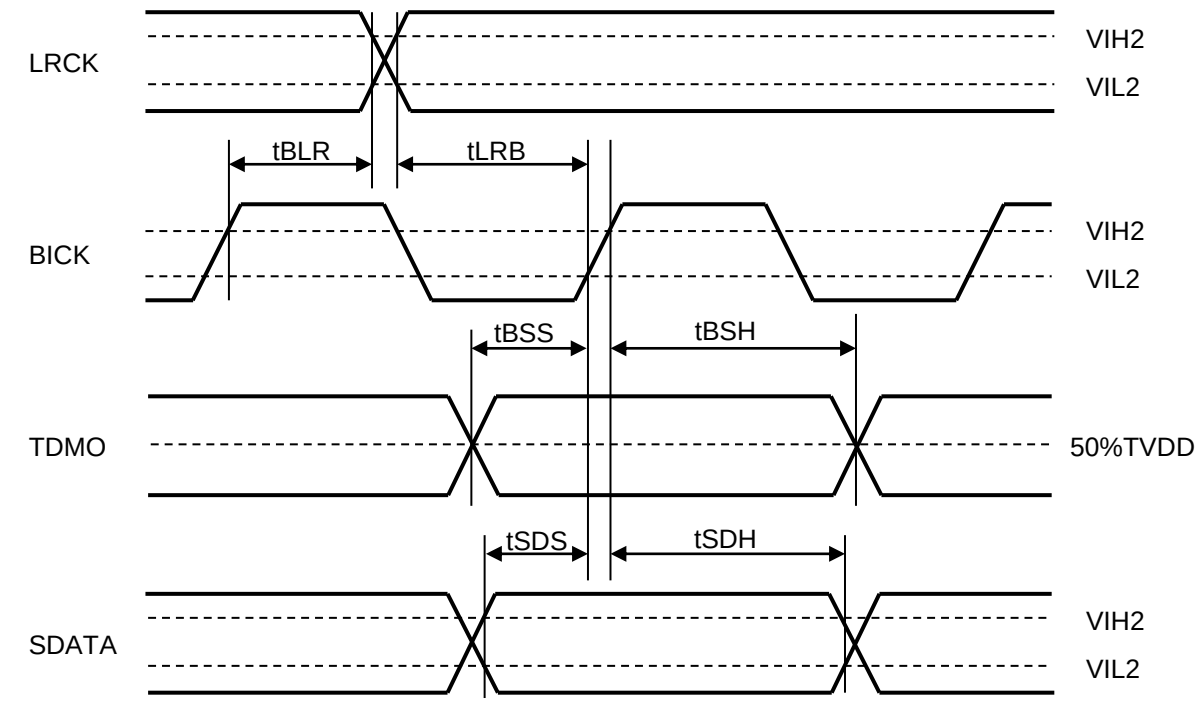


Figure 14. Audio Serial Data Interface Timing (PCM mode)

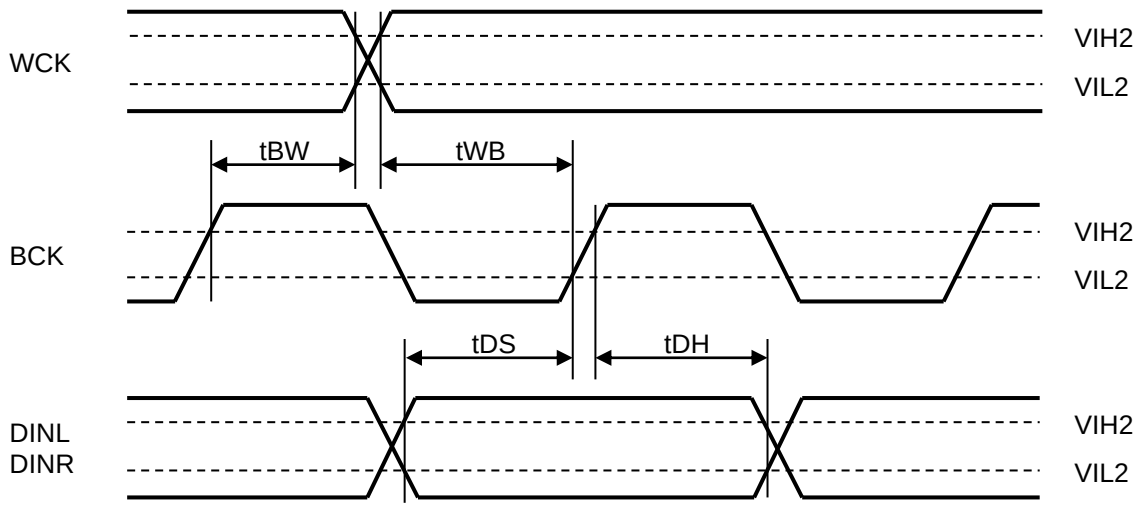
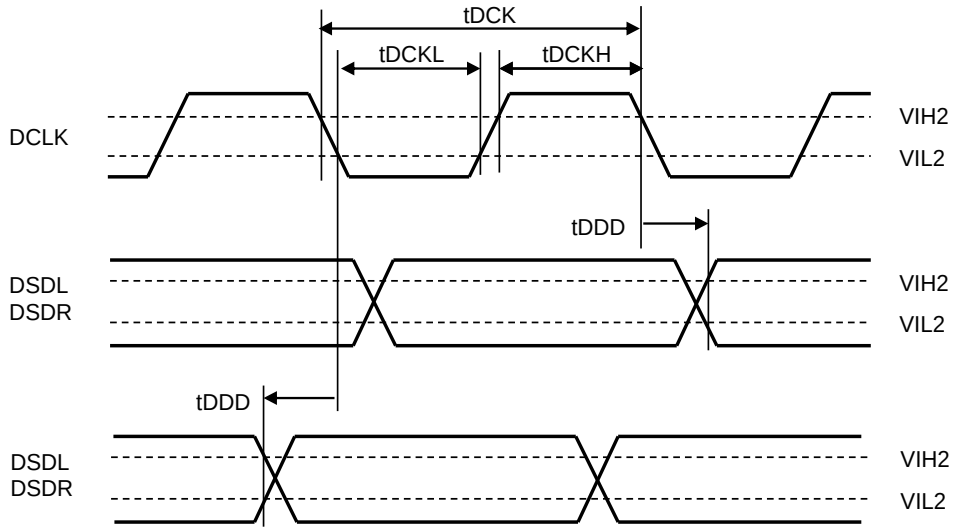
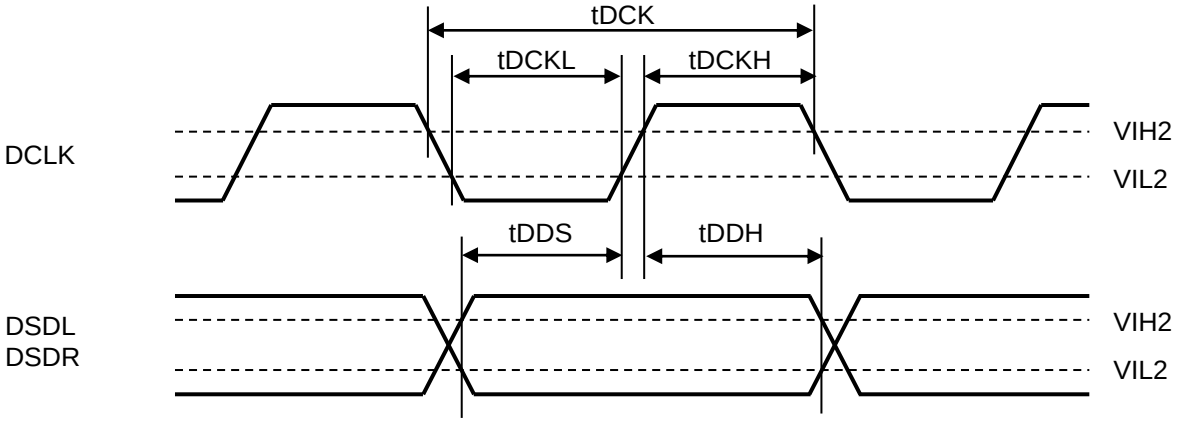


Figure 15. Audio Serial Data Interface Timing (EXDF mode)



DSD Audio Serial Data Interface Timing (DSD64, DSD128, DSD256 mode)



DSD Audio Serial Data Interface Timing (DSD512 mode)

Figure 16. Audio Serial Data Interface Timing (DSD Normal mode, DCKB bit = “0”)

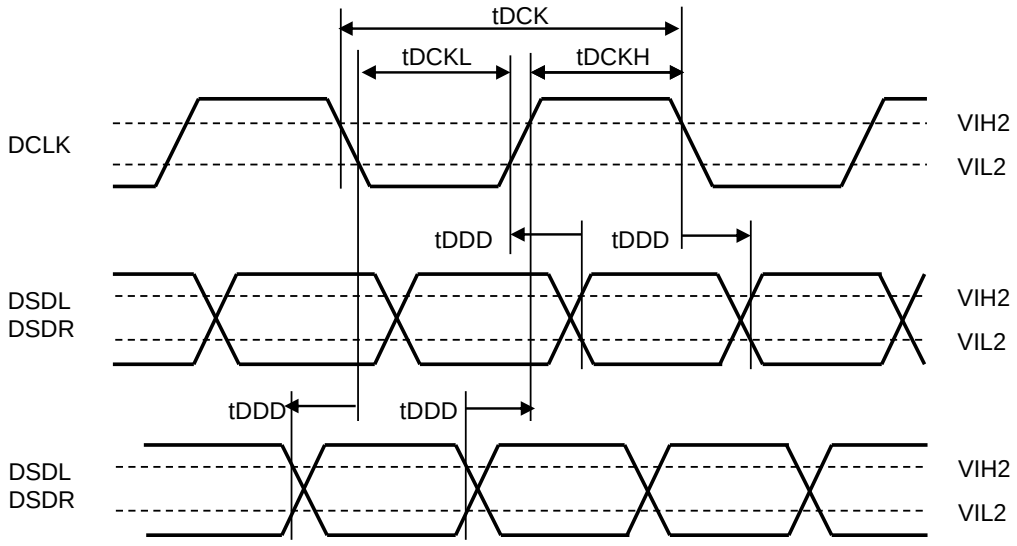


Figure 17. Audio Serial Data Interface Timing (DSD Phase Modulation mode, DCKB bit = “0”)

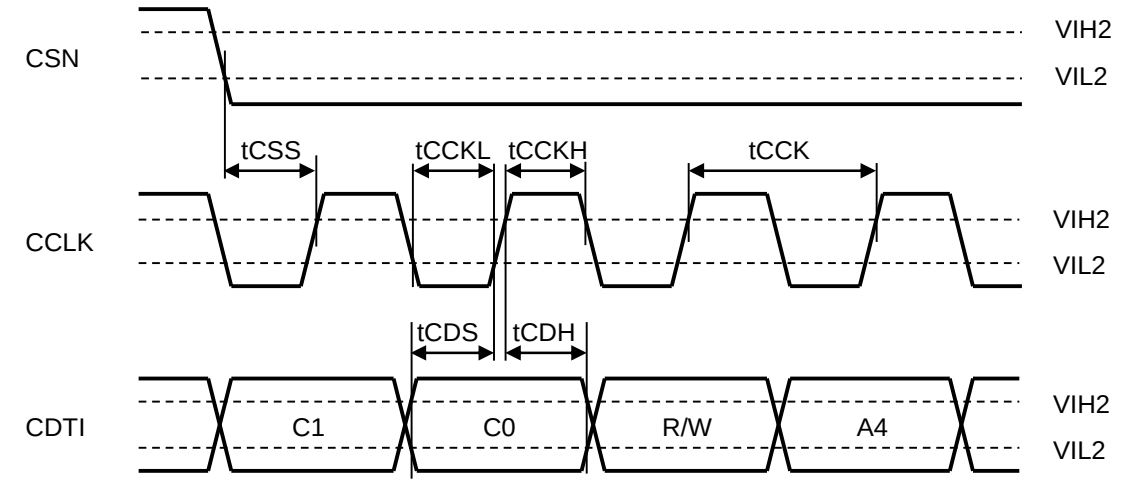


Figure 18. 3-wire Serial Interface Timing 1

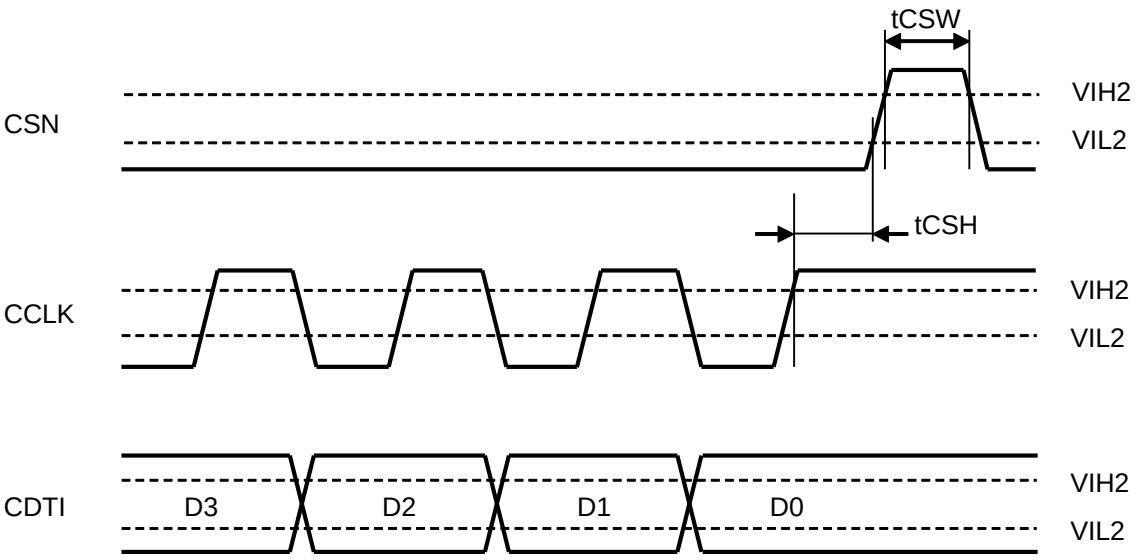


Figure 19. 3-wire Serial Interface Timing 2

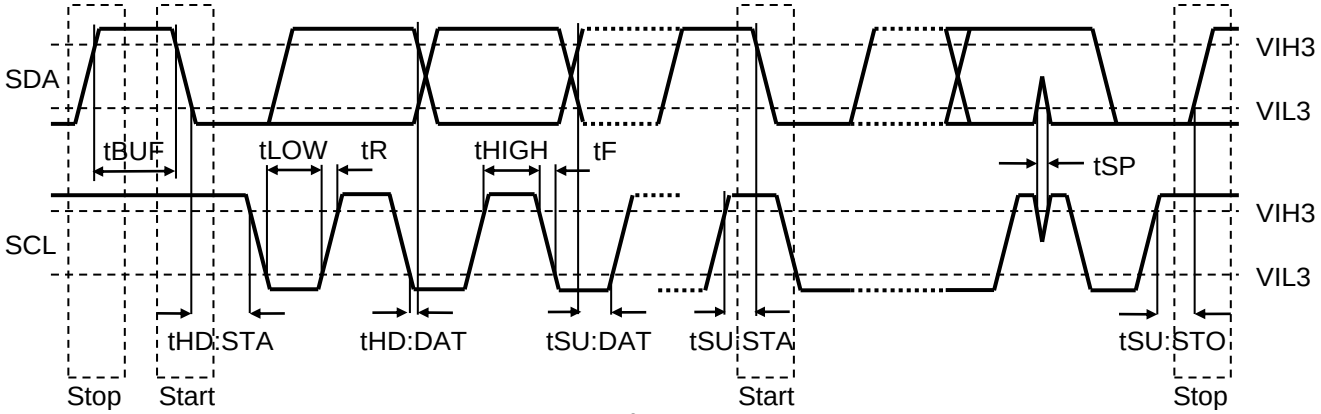


Figure 20. I²C-bus Timing

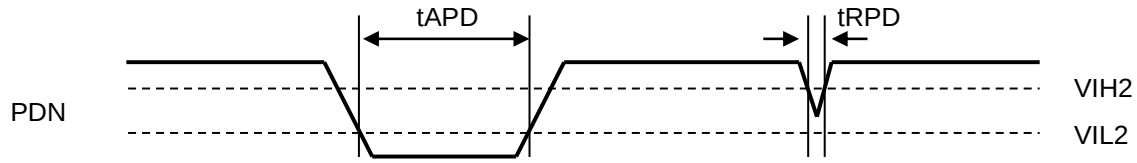


Figure 21. Power Down & Reset Timing

9. Functional Descriptions

9.1. Control Mode

Each function of the AK4497S is controlled by pins (Pin Control mode) or registers (Register Control mode). Select the control mode by PSN pin (Table 1). The AK4497S must be powered down by PDN pin when changing the PSN pin setting. There is a possibility of malfunction if the device is not powered down when changing the control mode since the previous setting is not reinitialized. Register settings are invalid in Pin Control mode, and pin settings are invalid in Register Control mode.

Table 2 shows available functions of each control mode and Table 3 shows available functions in each D/A conversion mode (PCM/DSD/EXDF).

Table 1. Pin/Register Control Mode Select

PSN pin	Control Mode
L	Register Control mode
H	Pin Control mode

Table 2. Function List in Register/Pin Control mode
(Y: Available, N/A: Not available)

Function	Register Control mode	Pin Control mode	
D/A Conversion Mode Select (PCM/DSD/EXDF mode)	Y	N/A	PCM mode only
System Clock Setting Mode Select	Y	Y	-
Audio Format Select	Y	Y	-
TDM Mode Select	Y	Y	-
Digital Filter Select	Y	Y	-
De-emphasis Filter Select	Y	Y	44.1 kHz only
Digital Attenuation Level Setting	Y	N/A	Fixed to 0 dB
Zero Detect	Y	N/A	-
Mono Mode	Y	N/A	Stereo only
Output Signal Channel Select (Monaural, Channel Swap)	Y	N/A	-
Output Signal Polarity Select (Invert)	Y	Y	Rch only
Sound Quality Select	Y	N/A	Same as SC[2:0] bits = “000”
DSD Full-Scale Detect	Y	N/A	-
Soft Mute	Y	Y	-
Reset by RSTN bit	Y	N/A	Released
On/Off Control of standby by stopping MCLK	Y	N/A	Always ON
On/Off Control of Clock Synchronization Function	Y	N/A	Always ON
Gain Control	Y	Y	2.8 Vpp or 3.75 Vpp
Heavy Load mode Select	Y	Y	-

Table 3. Function List of PCM/EXDF/DSD mode in Register Control mode
(Y: Available, N/A: Not available)

Function	Default State	Address	Register Name	PCM mode	EXDF mode	DSD mode	
						Normal	Volume Bypass
Automatic Conversion Mode Switching (PCM/DSD, EXDF/DSD)	Disable	15H	ADPE	Y	Y	Y	Y
Manual Conversion Mode Select (PCM, DSD, EXDF)	PCM mode	00H 02H	EXDF DP	Y	Y	Y	Y
DSD Path Select	Normal Path	06H	DSDD	N/A	N/A	Y	Y
System Clock Setting Mode Select @ PCM mode	Manual Setting mode	00H	ACKS	Y	N/A	N/A	N/A
MCLK Frequency Select @ DSD mode	512fsb	02H	DCKS	N/A	N/A	Y	Y
WCK Frequency Select @ EXDF mode	768 kHz	00H	ECS	N/A	Y	N/A	N/A
Digital Filter Select @ PCM mode	Short Delay Sharp Roll-off Filter	01H 02H 05H	SD SLOW SSLOW	Y (Note 48)	N/A	N/A	N/A
Digital Filter Select @ DSD mode	39 kHz Filter	09H	DSDF	N/A	N/A	Y	N/A
De-emphasis Response	OFF	01H	DEM[1:0]	Y	N/A	N/A	N/A
Audio Serial Data Interface Format Select @ PCM mode	32-bit MSB	00H	DIF[2:0]	Y	N/A	N/A	N/A
Audio Serial Data Interface Format Select @ EXDF mode	24-bit LSB	00H	DIF[2:0]	N/A	Y	N/A	N/A
TDM Interface Format Select	Normal mode	0AH	TDM[1:0]	Y	N/A	N/A	N/A
Daisy Chain	Normal mode	0BH	DCHAIN	Y	N/A	N/A	N/A
Digital Attenuator Attenuation Level Setting	0 dB	03-04H	ATTL[7:0] ATTR[7:0]	Y	Y	Y	N/A
Gain Control	2.8 Vpp	07H	GC[2:0]	Y	Y	Y	N/A
Zero Detection	Disable	01H	DZFE	Y	Y	Y	N/A
Inverting Polarity of DZFL/R pins	“H” at detecting zero	02H	DZFB	Y	Y	Y	Y
Mono/Stereo mode Select	Stereo	02H	MONO	Y	Y	Y	Y
Analog Output Polarity Invert	OFF	05H	INVL/R	Y	Y	Y	Y
Data Selection of L-channel and R-channel	Not Swap (Stereo) Rch (Mono)	02H	SELLR	Y	Y	Y	Y
Sound Quality Select	Setting 1 & Setting 3	08H	SC[2:0]	Y	Y	Y	Y
DSD Mute Function when Full-Scale Data Input	Disable	06H	DDM	N/A	N/A	Y	Y
Soft Mute Enable	Not Muted	01H	SMUTE	Y	Y	Y	N/A
RSTN	Reset	00H	RSTN	Y	Y	Y	Y
Clock Synchronization Function	Enable	07H	SYNCE	Y	Y	N/A	N/A

Note 48. In Oct Speed mode and Hex Speed mode, the digital filter is Super slow roll-off filter regardless of the filter setting.

9.2. D/A Conversion Mode (PCM mode, DSD mode, EXDF mode)

The AK4497S can convert either PCM or DSD data to an analog signal, and an external digital filter (EXDF) interface can also be selected. In PCM mode, PCM data can be input from the BICK, LRCK and SDATA pins. In DSD mode, DSD data can be input from the DCLK1, DSDL1 and DSDR1 pins or the DCLK2, DSDL2 and DSDR2 pins. When the DSDPATH bit = “0”, the DCLK2, DSDL2 and DSDR2 pins are enabled, and when the DSDPATH bit = “1", the DCLK1, DSDL1 and DSDR1 pins are enabled. In EXDF mode, an external digital filter output data can be input from the BCK, DINL, DINR and WCK pins. The AK4497S only supports PCM mode in Pin Control mode.

9.2.1. Manual Setting of D/A Conversion Mode (ADPE bit = “0”)

When the ADPE bit = “0”, select the D/A conversion mode with the DP and EXDF bits. The D/A conversion mode must be changed during reset state by setting the RSTN bit = “0”. The RSTN bit should not be changed for 4/fs after changing D/A conversion mode. It takes 2/fsb to 3/fsb for data mode switching. (Figure 23)

9.2.2. Auto Setting mode of D/A Conversion Mode (ADPE bit = “1”)

When the ADPE bit = “1”, D/A conversion mode will automatically switch between DSD mode and other modes regardless of the DP bit. PCM mode and EXDF mode must be manually set using the EXDF bit. The AK4497S monitors input signal of the LRCK/DSDR1 pin or the GAIN/DSDR2 pin to detect PCM or DSD mode when the EXDF bit = “0”, and it monitors input signal of the SSLOW/WCK pin to detect EXDF or DSD mode when the EXDF bit = “1”.

Table 4. D/A Conversion Mode Setting in Register Control mode

ADPE bit	DP bit	EXDF bit	D/A Conversion. Mode	
0	0	0	PCM	(default)
	0	1	EXDF	
	1	*	DSD	
1	*	0	Auto (PCM or DSD)	
		1	Auto (EXDF or DSD)	

(*: Do not care)

9.2.3. D/A Conversion Mode Switching Timing (Manual Setting)

Figure 22 and Figure 23 show switching timing of PCM/EXDF and DSD modes. To prevent noise caused by excessive input, DSD signal should be input at least 4/fsb after setting the RSTN bit = "0" until the device is completely reset internally when the conversion mode is changed to DSD mode from PCM/EXDF mode.

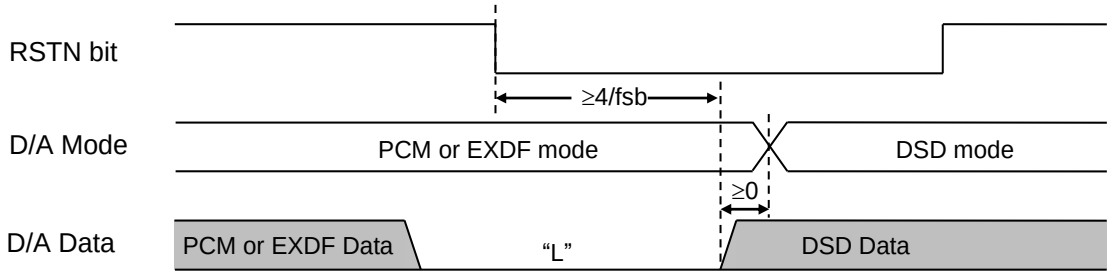


Figure 22. D/A Conversion Mode Switching Timing (from PCM/EXDF to DSD)

To prevent noise caused by excessive input, the DSD signal should be stopped at least 4/fsb after setting the RSTN bit = "0" until the device is completely reset internally when the conversion mode is changed to PCM/EXDF from DSD mode.

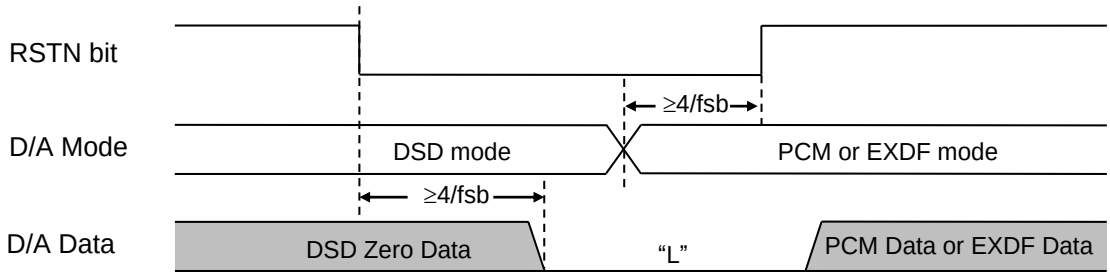


Figure 23. D/A Conversion Mode Switching Timing (from DSD to PCM/EXDF)

Figure 24 shows switching timing of PCM and EXDF modes. Set the EXDF bit at least 4/fsb after setting the RSTN bit = "0" until the device is completely reset internally when changing the conversion mode.

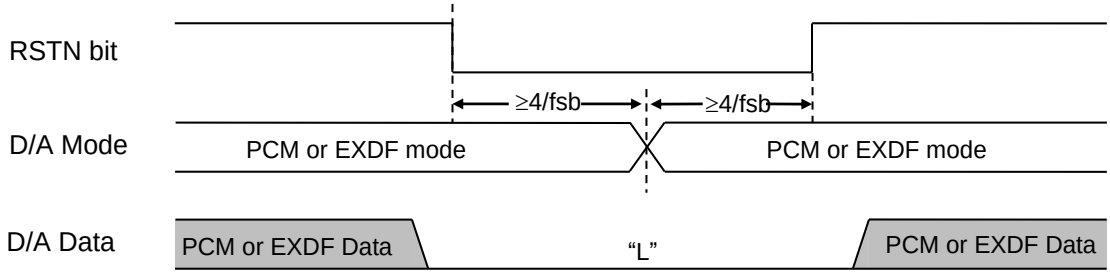


Figure 24. D/A Conversion Mode Switching Timing (from PCM to EXDF or from EXDF to PCM)

9.3. System Clock

9.3.1. PCM mode

The external clocks, which are required to operate the AK4497S, are MCLK, BICK and LRCK in PCM mode. MCLK, BICK and LRCK should be synchronized but the phase of MCLK is not critical. MCLK is used to operate the interpolator, the delta sigma modulator and SCF. There are Manual Setting mode, Auto Setting mode and fs Auto Detection mode for MCLK frequency setting. (Table 5).

In Manual Setting mode (ACKS pin = "L" or ACKS bit = "0"), the MCLK frequency is set automatically but the sampling speed (LRCK frequency) is set by the DFS2-0 bits (Table 10). The sampling speed is fixed to Normal Speed mode in Pin Control mode. In Register Control mode, the AK4497S is in Manual Setting mode when power down is released (PDN pin = "L" → "H").

In Auto Setting mode (ACKS pin = "H" or ACKS bit = "1"), the sampling speed and MCLK frequency are detected automatically (Table 7, Table 8, Table 13, Table 14) and the internal master clock is configured accordingly.

In fs Auto Detect mode (AFSD bit = "1"), the sampling speed is automatically detected (Table 16, Table 17) and the internal master clock is set to the appropriate frequency. In this mode, the ACKS bit and DFS[2:0] bits settings are invalid. Also, the automatic detection result can be checked by reading the ADFS[2:0] bits (Addr.15H D[2:0], read only). Fs Auto Detect mode is not supported in Pin Control mode.

The AK4497S is in standby state until MCLK, BICK and LRCK are supplied after PDN pin = H, and the analog output is in floating (Hi-Z) state. All circuits except for control registers, bias generation, and the internal LDO (if LDOE pin = "H") of the AK4497S are automatically placed in standby state when MCLK is stopped for more than 1 μs during normal operation (PDN pin = "H", MSTBN bit = "0"), and the analog output becomes floating (Hi-Z) state. When MCLK is input again, the AK4497S exits this standby state and starts operation again. In this case, register settings are not initialized.

Table 5. System Clock Setting Mode in Register Control mode (*: Do not Care)

AFSD bit	ACKS bit	System Clock Setting Mode	
0	0	Manual setting	(default)
	1	Auto setting	
1	*	fs Auto Detect	

9.3.1.1. Clock Setting in Pin Control mode (PSN pin = "H")

- Manual Setting mode (ACKS pin = "L")

MCLK must be provided at the frequency ratios shown in Table 6. The sampling speed mode is fixed to Normal Speed in Pin Control and Manual Setting modes. The Hex, Octal, Quad and Double Speed modes are not available.

Table 6. System Clock Example (Manual Setting mode @Pin Control mode)

LRCK	MCLK [MHz]								BICK
fs	128fs	192fs	256fs	384fs	512fs	768fs	1024fs	1152fs	64fs
32.0 kHz	N/A	N/A	8.1920	12.2880	16.3840	24.5760	32.7680	36.8640	2.0480 MHz
44.1 kHz	N/A	N/A	11.2896	16.9344	22.5792	33.8688	N/A	N/A	2.8224 MHz
48.0 kHz	N/A	N/A	12.2880	18.4320	24.5760	36.8640	N/A	N/A	3.0720 MHz

(N/A: Not available)

- Auto Setting mode (ACKS pin = “H”)

The MCLK frequency and sampling frequency are detected automatically. MCLK must be provided at the frequency ratios shown in Table 7 and Table 8.

Table 7. System Clock Example 1 (Auto Setting mode @Pin Control mode)

LRCK	MCLK Frequency [MHz]						Sampling Speed Mode
fs	32fs	48fs	64fs	96fs	128fs	192fs	
32.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Normal (≤ 32 kHz)
44.1 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Normal (> 32 kHz)
48.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	
88.2 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Double
96.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	
176.4 kHz	N/A	N/A	N/A	N/A	22.5792	33.8688	Quad
192.0 kHz	N/A	N/A	N/A	N/A	24.5760	36.8640	
384 kHz	N/A	N/A	24.576	36.864	N/A	N/A	Oct
768 kHz	24.576	36.864	N/A	N/A	N/A	N/A	Hex

(N/A: Not available)

Table 8. System Clock Example 2 (Auto Setting mode @Pin Control mode)

LRCK	MCLK Frequency [MHz]						Sampling Speed Mode
fs	256fs	384fs	512fs	768fs	1024fs	1152fs	
32.0 kHz	8.1920	12.2880	16.3840	24.5760	32.7680	36.8640	Normal (≤ 32 kHz)
44.1 kHz	11.2896	16.9344	22.5792	33.8688	N/A	N/A	Normal (> 32 kHz)
48.0 kHz	12.2880	18.4320	24.5760	36.8640	N/A	N/A	
88.2 kHz	22.5792	33.8688	N/A	N/A	N/A	N/A	Double
96.0 kHz	24.5760	36.8640	N/A	N/A	N/A	N/A	
176.4 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Quad
192.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	
384 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Oct
768 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Hex

(N/A: Not available)

When MCLK = 256fs or 384fs, Auto Setting mode supports sampling rates of 30 kHz to 96 kHz (Table 8). However, the dynamic range and S/N performances will degrade approximately 3 dB if the sampling rate is 44.1 kHz. It is due to the internal oversampling ratio being reduced by one half.

Table 9. Relationship between DR, S/N Degradation at fs=44.1kHz and MCLK Frequency

ACKS pin	MCLK Frequency	Dynamic Range, S/N (A-weighted)
L	256fs/384fs/512fs/768fs	129 dB
H	256fs/384fs	126 dB
H	512fs/768fs	129 dB

9.3.1.2. Clock Setting in Register Control mode (PSN pin = “L”)

- Manual Setting mode (AFSD bit = “0”, ACKS bit = “0”)

MCLK frequency is detected automatically, and the Sampling Speed Mode is set by DFS[2:0] bits (Table 10). MCLK must be provided at the frequency ratios shown in Table 11 and Table 12.

Table 10. Sampling Speed mode Setting (Manual Setting mode @Register Control mode)

DFS2 bit	DFS1 bit	DFS0 bit	Sampling Speed Mode	Sampling Rate (fs)	
0	0	0	Normal Speed mode	30 kHz to 54 kHz	(default)
0	0	1	Double Speed mode	54 kHz to 108 kHz	
0	1	*	Quad Speed mode	120 kHz to 216 kHz	
1	*	0	Oct Speed mode	216 kHz to 388 kHz	
1	*	1	Hex Speed mode	388 kHz to 776 kHz	

(*: Do not Care)

Table 11. System Clock Example 1 (Manual Setting mode @Register Control mode)

LRCK	MCLK Frequency [MHz]						Sampling Speed Mode
fs	16fs	32fs	48fs	64fs	96fs	128fs	
32.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Normal (≤ 32 kHz)
44.1 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Normal (> 32 kHz)
48.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	
88.2 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Double
96.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	
176.4 kHz	N/A	N/A	N/A	N/A	N/A	22.5792	Quad
192.0 kHz	N/A	N/A	N/A	N/A	N/A	24.5760	
384 kHz	N/A	12.288	18.432	24.576	36.864	N/A	Oct
768 kHz	12.288	24.576	36.864	49.152	N/A	N/A	Hex

(N/A: Not available)

Table 12. System Clock Example 2 (Manual Setting mode @Register Control mode)

LRCK	MCLK Frequency [MHz]							Sampling Speed Mode
fs	192fs	256fs	384fs	512fs	768fs	1024fs	1152fs	
32.0 kHz	N/A	8.1920	12.2880	16.3840	24.5760	32.7680	36.8640	Normal (≤ 32 kHz)
44.1 kHz	N/A	11.2896	16.9344	22.5792	33.8688	N/A	N/A	Normal (> 32 kHz)
48.0 kHz	N/A	12.2880	18.4320	24.5760	36.8640	N/A	N/A	
88.2 kHz	N/A	22.5792	33.8688	45.1584	N/A	N/A	N/A	Double
96.0 kHz	N/A	24.5760	36.8640	49.152	N/A	N/A	N/A	
176.4 kHz	33.8688	45.1584	N/A	N/A	N/A	N/A	N/A	Quad
192.0 kHz	36.8640	49.152	N/A	N/A	N/A	N/A	N/A	
384 kHz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Oct
768 kHz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Hex

(N/A: Not available)

The AK4497S is in Manual Setting mode at power up default (PDN pin = “L” → “H”). When the DFS[2:0] bits are changed, the AK4497S should be reset by the RSTN bit.

・ Auto Setting mode (AFSD bit = “0”, ACKS bit = “1”)

MCLK frequency and the sampling speed are detected automatically and the DFS[2:0] bits are ignored. MCLK must be provided at the frequency ratios shown in Table 13 and Table 14.

Table 13. System Clock Example 1 (Auto Setting mode @Register Control mode)

LRCK	MCLK Frequency [MHz]						Sampling Speed Mode
fs	32fs	48fs	64fs	96fs	128fs	192fs	
32.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Normal (≤ 32 kHz)
44.1 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Normal (> 32 kHz)
48.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	
88.2 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Double
96.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	
176.4 kHz	N/A	N/A	N/A	N/A	22.5792	33.8688	Quad
192.0 kHz	N/A	N/A	N/A	N/A	24.5760	36.8640	
384 kHz	N/A	N/A	24.576	36.864	N/A	N/A	Oct
768 kHz	24.576	36.864	N/A	N/A	N/A	N/A	Hex

(N/A: Not available)

Table 14. System Clock Example 2 (Auto Setting mode @Register Control mode)

LRCK	MCLK Frequency [MHz]						Sampling Speed Mode
fs	256fs	384fs	512fs	768fs	1024fs	1152fs	
32.0 kHz	8.1920	12.2880	16.3840	24.5760	32.7680	36.8640	Normal (≤ 32 kHz)
44.1 kHz	11.2896	16.9344	22.5792	33.8688	N/A	N/A	Normal (> 32 kHz)
48.0 kHz	12.2880	18.4320	24.5760	36.8640	N/A	N/A	
88.2 kHz	22.5792	33.8688	N/A	N/A	N/A	N/A	Double
96.0 kHz	24.5760	36.8640	N/A	N/A	N/A	N/A	
176.4 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Quad
192.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	
384 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Oct
768 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Hex

(N/A: Not available)

When MCLK = 256fs/384fs, Auto Setting mode supports sampling rates of 30 kHz to 96 kHz (Table 14). However, the dynamic range and S/N performances will degrade approximately 3 dB if the sampling rate is 44.1 kHz. It is due to the internal oversampling ratio being reduced by one half.

Table 15. Relationship between DR, S/N Degradation at fs = 44.1kHz and MCLK Frequency

ACKS bit	MCLK Frequency	Dynamic Range, S/N (A-weighted)
L	256fs/384fs/512fs/768fs	129 dB
H	256fs/384fs	126 dB
H	512fs/768fs	129 dB

・ Sampling Frequency (fs) Auto Detect mode (AFSD bit = “1”, ACKS bit = Don’t Care)

MCLK frequency and the sampling rate is detected automatically. In fs Auto Detect mode, the DFS[2:0] bits and ACKS bit settings are invalid. MCLK must be provided at the frequency ratios shown in Table 16 and Table 17. Figure 25 and Figure 26 show the fs Auto Detect mode switching sequence.

Table 16. System Clock Example 1 (fs Auto Detect mode @Register Control mode)

LRCK	MCLK Frequency [MHz]						Sampling Speed Mode
fs	16fs	32fs	48fs	64fs	96fs	128fs	
32.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Normal (≤ 32 kHz)
44.1 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Normal (> 32 kHz)
48.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	
88.2 kHz	N/A	N/A	N/A	N/A	N/A	N/A	Double
96.0 kHz	N/A	N/A	N/A	N/A	N/A	N/A	
176.4 kHz	N/A	N/A	N/A	N/A	N/A	22.5792	Quad
192.0 kHz	N/A	N/A	N/A	N/A	N/A	24.5760	
384 kHz	N/A	12.288	18.432	24.576	36.864	N/A	Oct
768 kHz	12.288	24.576	36.864	49.152	N/A	N/A	Hex

(N/A: Not available)

Table 17. System Clock Example 2 (fs Auto Detect mode @Register Control mode)

LRCK	MCLK Frequency [MHz]							Sampling Speed Mode
fs	192fs	256fs	384fs	512fs	768fs	1024fs	1152fs	
32.0 kHz	N/A	8.1920	12.2880	16.3840	24.5760	32.768	36.8640	Normal (≤ 32 kHz)
44.1 kHz	N/A	11.2896	16.9344	22.5792	33.8688	N/A	N/A	Normal (> 32 kHz)
48.0 kHz	N/A	12.2880	18.4320	24.5760	36.8640	N/A	N/A	
88.2 kHz	N/A	22.5792	33.8688	45.1584	N/A	N/A	N/A	Double
96.0 kHz	N/A	24.5760	36.8640	49.152	N/A	N/A	N/A	
176.4 kHz	33.8688	45.1584	N/A	N/A	N/A	N/A	N/A	Quad
192.0 kHz	36.8640	49.152	N/A	N/A	N/A	N/A	N/A	
384 kHz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Oct
768 kHz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Hex

(N/A: Not available)

The automatic detection result can be read out form the ADFS[2:0] bits.

Table 18. fs Auto Detection Result (fs Auto Detect mode @Register Control mode)

ADFS2 bit	ADFS1 bit	ADFS0 bit	Sampling Speed Mode
0	0	0	Normal Speed mode (default)
0	0	1	Double Speed mode
0	1	0	Quad Speed mode
1	0	0	Oct Speed mode
1	0	1	Hex Speed mode

<Switching to fs Auto Detect mode>

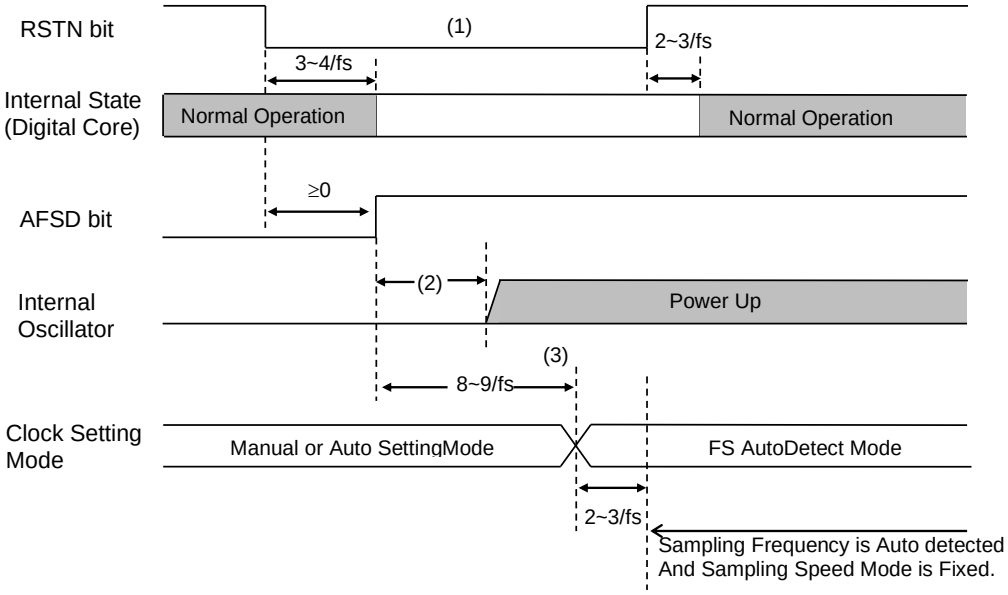


Figure 25. Switching to fs Auto Detect mode

Notes:

(1) Digital block of the AK4497S should be reset when changing the clock setting mode.
(2) The internal oscillator starts operation by setting the AFSD bit = “1”. It takes 10 μs (max.) until the internal oscillator is stabilized.
(3) The fs Auto Detect mode starts in 8/fs to 9/fs after setting the AFSD bit = “1”. Internal operation rate will be stabilized in 2/fs to 3/fs. The digital block should be in reset state until the internal operation rate is stabilized.

<Switching to other Clock Setting Mode from fs Auto Detect mode>

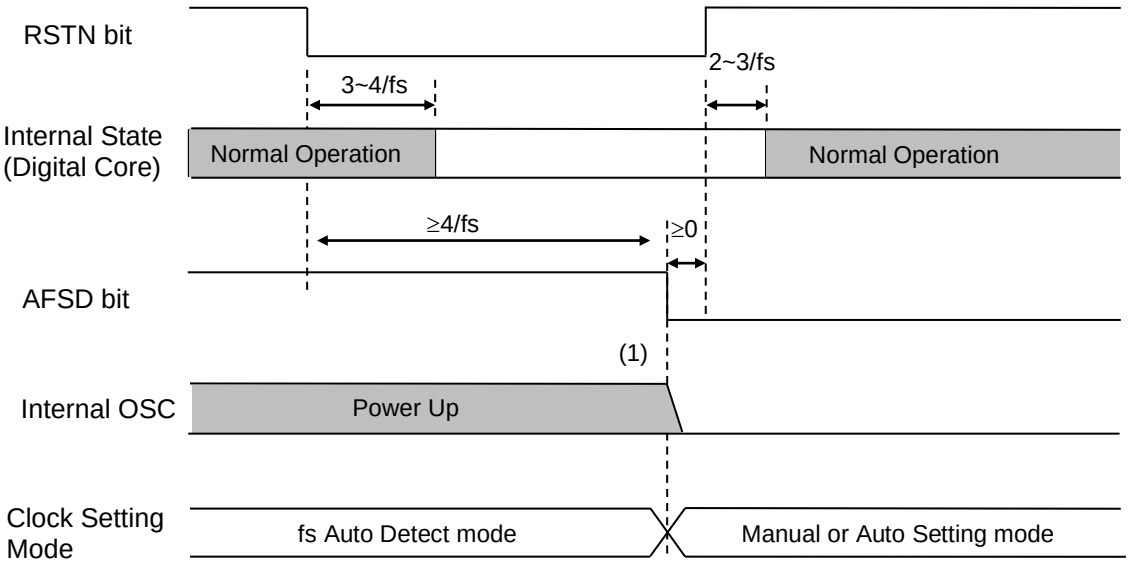


Figure 26. Switching from fs Auto Detect mode

Note:

(1) The fs Auto Detect mode ends by setting the AFSD bit = “0” and the internal oscillator will stop operation.

9.3.2. DSD mode

The AK4497S has a DSD playback function. The external clocks that are required in DSD mode are MCLK and DCLK. MCLK should be synchronized with DCLK, but the phase is not critical. The frequency of MCLK is set by the DCKS bit (Table 19).

The AK4497S is automatically placed in standby state when MCLK is stopped during normal operation (PDN pin = "H", MSTBN bit = "0"), and the analog output becomes Hi-Z state. When the power down is released (PDN pin = "L" → "H"), the AK4497S is in standby state until MCLK and DCLK are input.

Table 19. System Clock (DSD mode, fsb=32 kHz, 44.1 kHz, 48 kHz)

DCKS bit	MCLK Frequency	DCLK Frequency	
0	512fsb	64fsb/128fsb/256fsb/512fsb	(default)
1	768fsb	64fsb/128fsb/256fsb/512fsb	

The AK4497S supports DSD data stream frequency of 64fsb, 128fsb, 256fsb and 512fsb. The data stream frequency is selected by the DSDSEL[1:0] bits (Table 20). The DSDSEL[1:0] bits are changed during RSTN bit = "0".

Table 20. DSD Data Stream Frequency Select

Mode Name	DSDSEL1 bit	DSDSEL0 bit	DCLK Frequency	Data Stream Frequency			
				fsb = 32 kHz	fsb = 44.1 kHz	fsb = 48 kHz	
DSD64	0	0	64fsb	2.048 MHz	2.8224 MHz	3.072 MHz	(default)
DSD128	0	1	128fsb	4.096 MHz	5.6448 MHz	6.144 MHz	
DSD256	1	0	256fsb	8.192 MHz	11.2896 MHz	12.288 MHz	
DSD512	1	1	512fsb	16.384 MHz	22.5792 MHz	24.576 MHz	

9.3.3. External Digital Filter (EXDF) mode

The external clocks that are required in EXDF mode are MCLK, BCK and WCK. The BCK and MCLK must be the same frequency and continuous (not burst). BCK and MCLK frequencies for each sampling frequency are shown in Table 21. The ECS bit selects WCK frequency from 384 kHz and 768 kHz.

All circuits except for control registers, bias generation circuit and the internal LDO (if LDOE pin = "H") of the AK4497S are automatically placed in standby state when MCLK edge is not detected for more than 1 μs during normal operation (PDN pin = "H", MSTBN bit = "0"), and the analog output becomes Hi-Z state. The standby state is released and the AK4497S starts operation by inputting MCLK again. In this case, register settings are not initialized.
When the reset pin is released (PDN pin = "L" → "H"), the AK4497S remains in power down state until MCLK, BCK and WCK are input.

Table 21. System Clock Example (EXDF mode) (N/A: Not available)

ECS bit	WCK Frequency [kHz]	MCLK & BCK [MHz]				
	fs	32fs	48fs	64fs	96fs	
1	352.8	11.2896	16.9344	22.5792	33.8688	
	384	12.288	18.432	24.576	36.864	
0	705.6	22.5792	33.8688	N/A	N/A	(default)
	768	24.576	36.864	N/A	N/A	

9.4. Audio Serial Data Interface

9.4.1. PCM mode

9.4.1.1. Data Format

Audio serial data is shifted in via the SDATA pin using the BICK and LRCK inputs. The data is latched on the rising edge of BICK. The data is MSB first, 2's complement. The data format is selected by the TDM1-0 pins and DIF2–0 pins (Pin Control mode) or the TDM[1:0] bits and DIF[2:0] bits (Register Control mode) as shown in Table 22. Fill the unused bits with "0" if the data does not use the full bit length in MSB justified or I^{2}S compatible format (e.g., 24-bit MSB justified format can be used for 16-bit data by zeroing the unused lower 8 bits). The data format should not be changed during operation.

Normal mode (TDM[1:0] bits = "00" or TDM1-0 pins = "LL")
2-ch data is shifted in via the SDATA pin. Eight data formats are supported as shown in Table 22. The number of BICK cycles included in one LRCK cycle must be at least twice the bit length of each format. The maximum number of BICK cycles is determined by the BICK period (min. tBCK) in the switching characteristics. In 16-bit I^{2}S compatible format, the BICK number must be exactly 32 clocks.

TDM128 mode (TDM[1:0] bits = "01" or TDM1-0 pins = "LH")
4-ch Data is shifted in via the SDATA pin. Select the 2-ch data slot to be used with the SDS[2:0] bits (Table 23). BICK is fixed to 128fs. Six data formats are supported as shown in Table 22.

TDM256 mode (TDM[1:0] bits = "10" or TDM1-0 pins = "HL")
8-ch Data is shifted in via the SDATA pin. Select the 2-ch data slot to be used with the SDS[2:0] bits (Table 23). BICK is fixed to 256fs. Six data formats are supported as shown in Table 22.

TDM512 mode (TDM[1:0] bits = "11" or TDM1-0 pins = "HH")
16-ch Data is shifted in via the SDATA pin. Select the 2-ch data slot to be used with the SDS[2:0] bits (Table 23). BICK is fixed to 512fs. Six data formats are supported as shown in Table 22.

Table 22. Audio Serial Data Interface Format

Input Mode	TDM1 bit/pin	TDM0 bit/pin	Mode	DIF2 bit/pin	DIF1 bit/pin	DIF0 bit/pin	Data Format	LRCK	BICK	Figure	
Normal (Note 49)	0	0	0	0	0	0	16-bit LSB justified	H/L	≥32fs	Figure 27	
			1	0	0	1	20-bit LSB justified	H/L	≥40fs	Figure 28	
			2	0	1	0	24-bit MSB justified	H/L	≥48fs	Figure 29	
			3	0	1	1	16-bit I²S compatible	L/H	32fs	Figure 30	
							24-bit I²S compatible	L/H	≥48fs		
			4	1	0	0	24-bit LSB justified	H/L	≥48fs	Figure 28	
			5	1	0	1	32-bit LSB justified	H/L	≥64fs	Figure 31	
			6	1	1	0	32-bit MSB justified	H/L	≥64fs	Figure 32	(default)
			7	1	1	1	32-bit I²S compatible	L/H	≥64fs	Figure 33	
TDM128	0	1	8	0	1	0	24-bit MSB justified	H/L	128fs	Figure 34	
			9	0	1	1	24-bit I²S compatible	L/H	128fs	Figure 35	
			10	1	0	0	24-bit LSB justified	H/L	128fs	Figure 36	
			11	1	0	1	32-bit LSB justified	H/L	128fs	Figure 34	
			12	1	1	0	32-bit MSB justified	H/L	128fs	Figure 34	
			13	1	1	1	32-bit I²S compatible	L/H	128fs	Figure 35	
TDM256	1	0	14	0	1	0	24-bit MSB justified	H/L	256fs	Figure 37	
			15	0	1	1	24-bit I²S compatible	L/H	256fs	Figure 38	
			16	1	0	0	24-bit LSB justified	H/L	256fs	Figure 39	
			17	1	0	1	32-bit LSB justified	H/L	256fs	Figure 37	
			18	1	1	0	32-bit MSB justified	H/L	256fs	Figure 37	
			19	1	1	1	32-bit I²S compatible	L/H	256fs	Figure 38	
TDM512	1	1	20	0	1	0	24-bit MSB justified	H/L	512fs	Figure 40	
			21	0	1	1	24-bit I²S compatible	L/H	512fs	Figure 41	
			22	1	0	0	24-bit LSB justified	H/L	512fs	Figure 42	
			23	1	0	1	32-bit LSB justified	H/L	512fs	Figure 40	
			24	1	1	0	32-bit MSB justified	H/L	512fs	Figure 40	
			25	1	1	1	32-bit I²S compatible	L/H	512fs	Figure 41	

Note 49. In the LRCK column, “H/L” means that the “H” period of LRCK indicates L channel data, and the “L” period indicates R channel data. Similarly, “L/H” means that the “L” period of LRCK indicates L channel data, and the “H” period indicates R channel data.

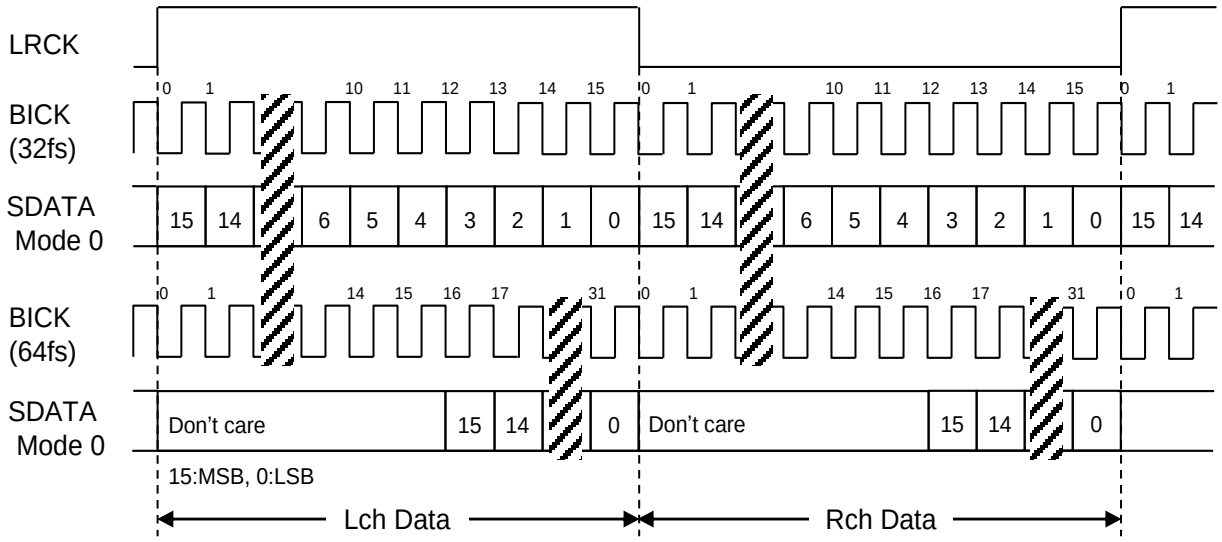


Figure 27. 16-bit LSB justified (Mode 0) Timing

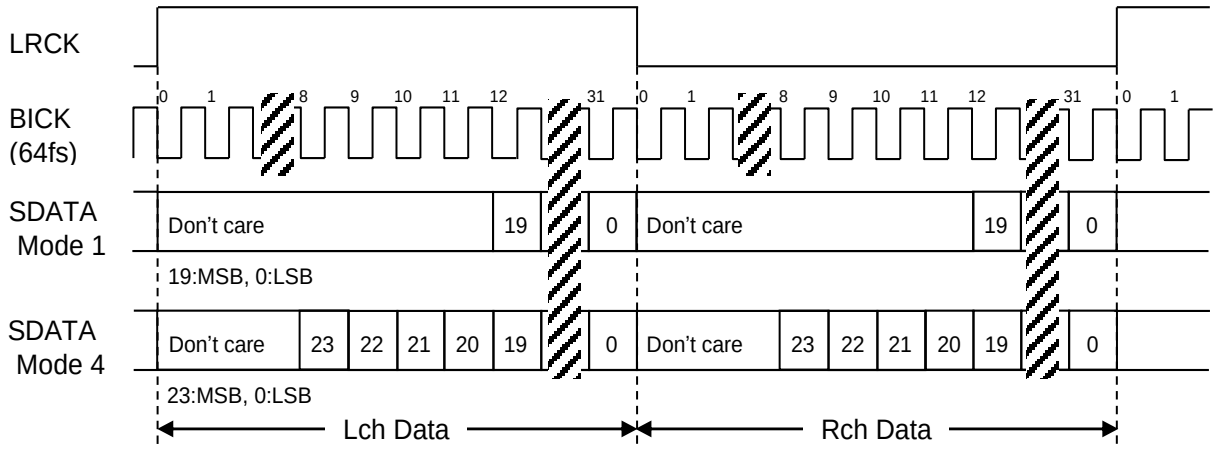


Figure 28. 20-bit, 24-bit LSB justified (Mode 1, 4) Timing

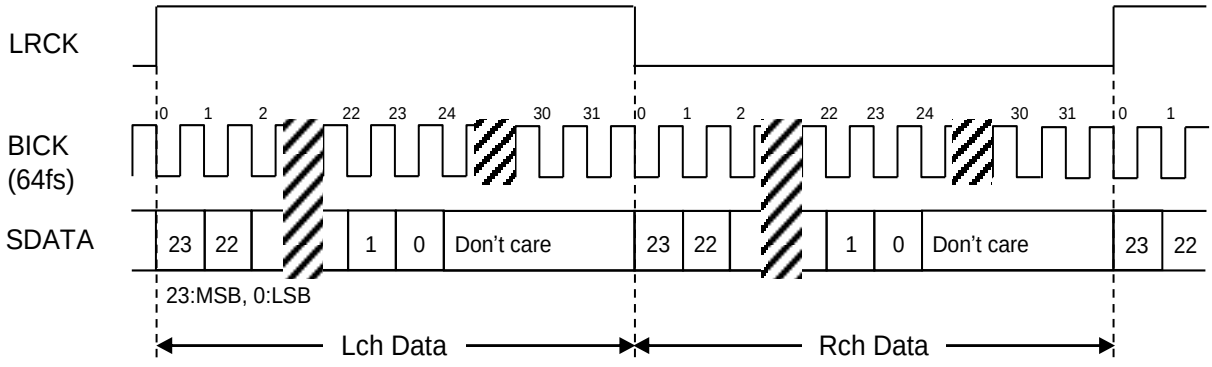


Figure 29. 24-bit MSB justified (Mode 2) Timing

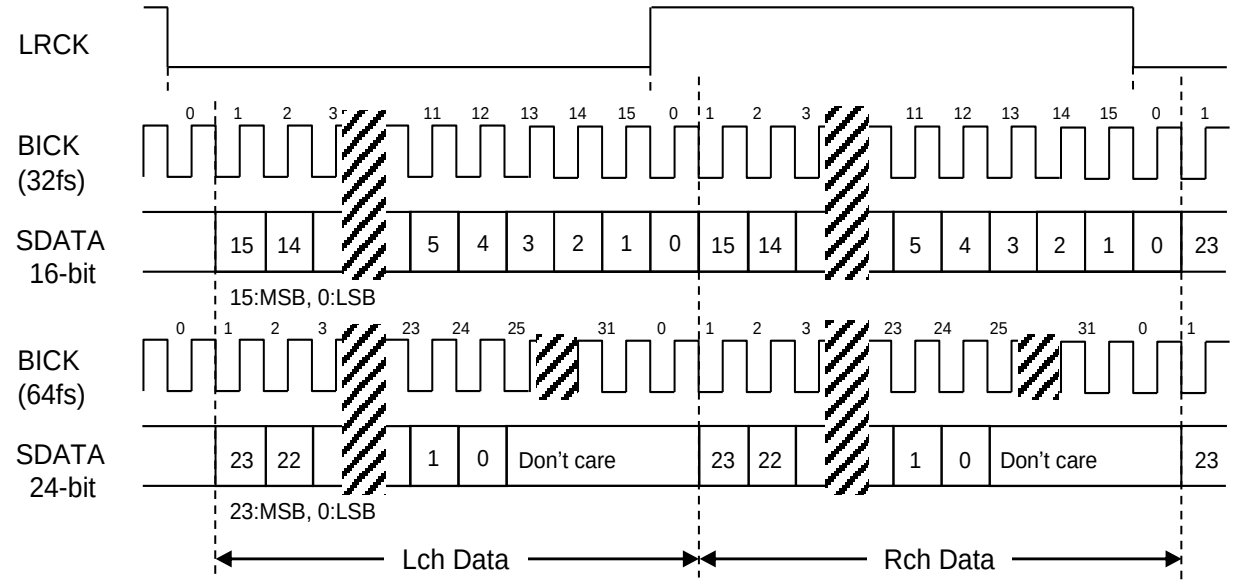


Figure 30. 16-bit/24-bit I²S compatible (Mode 3) Timing

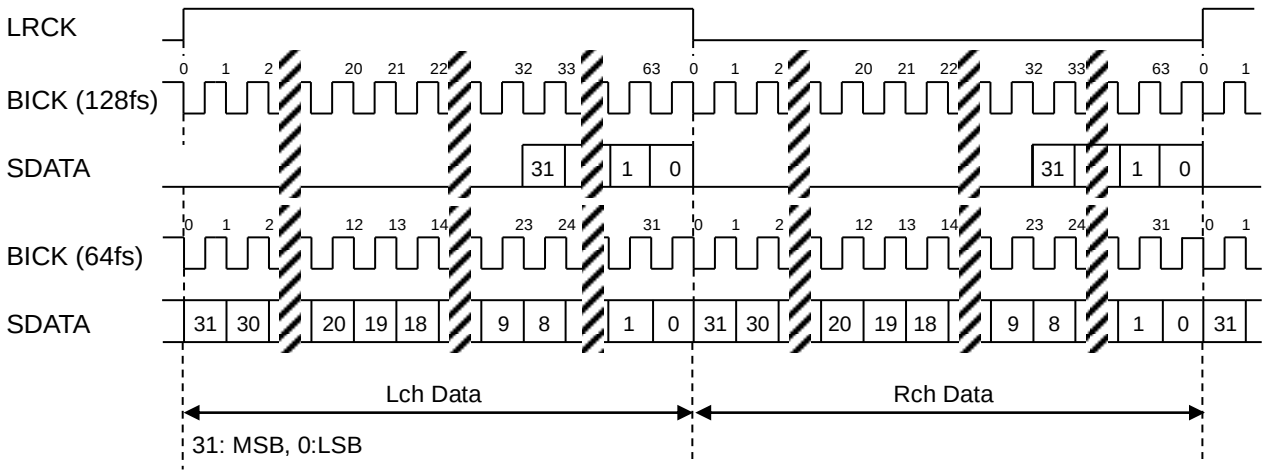


Figure 31. 32-bit LSB justified (Mode 5) Timing

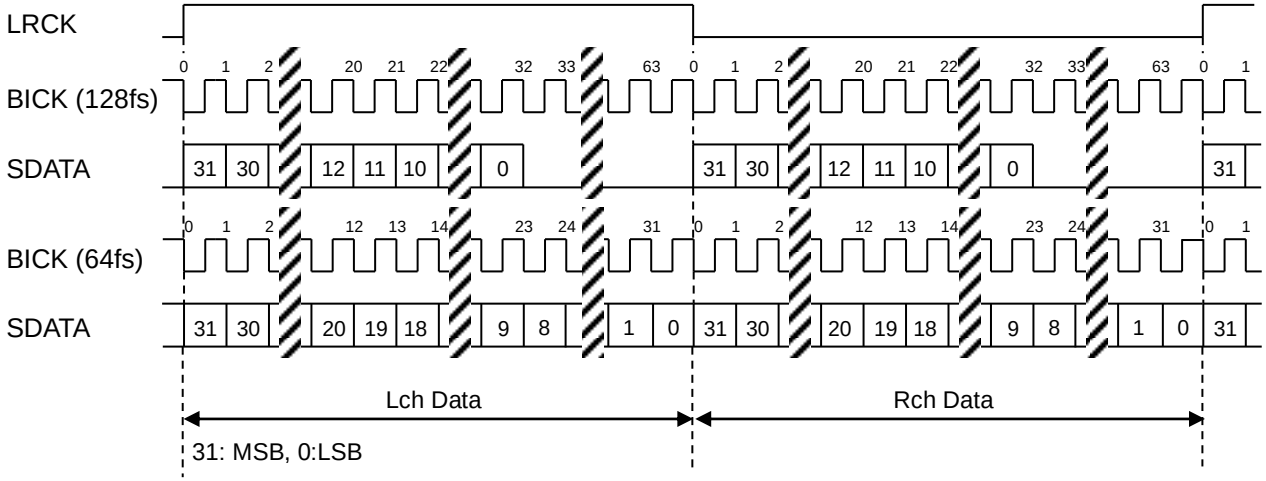


Figure 32. 32-bit MSB justified (Mode 6) Timing

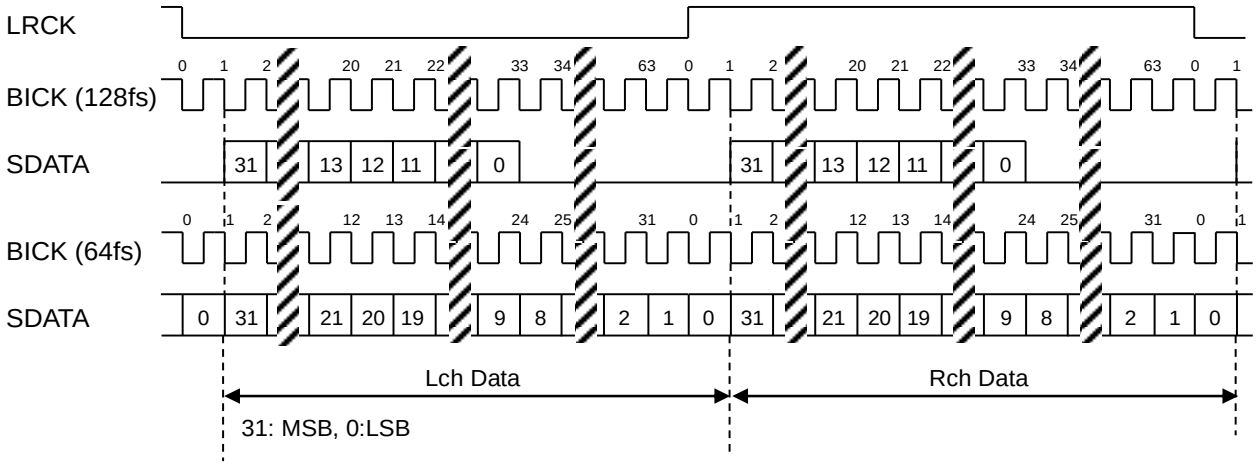


Figure 33. 32-bit I²S compatible (Mode 7) Timing

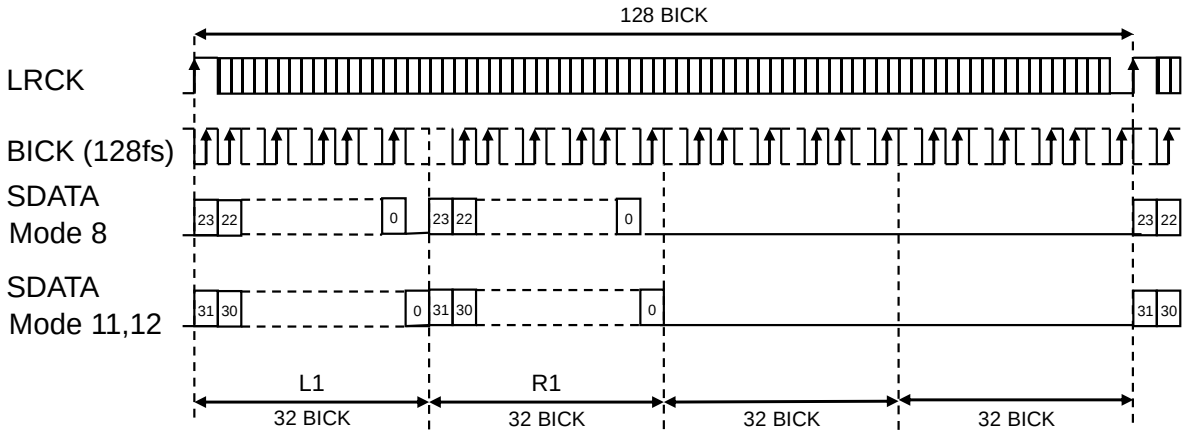


Figure 34. TDM128, 24-bit MSB justified, 32-bit MSB/LSB justified (Mode 8/11/12) Timing

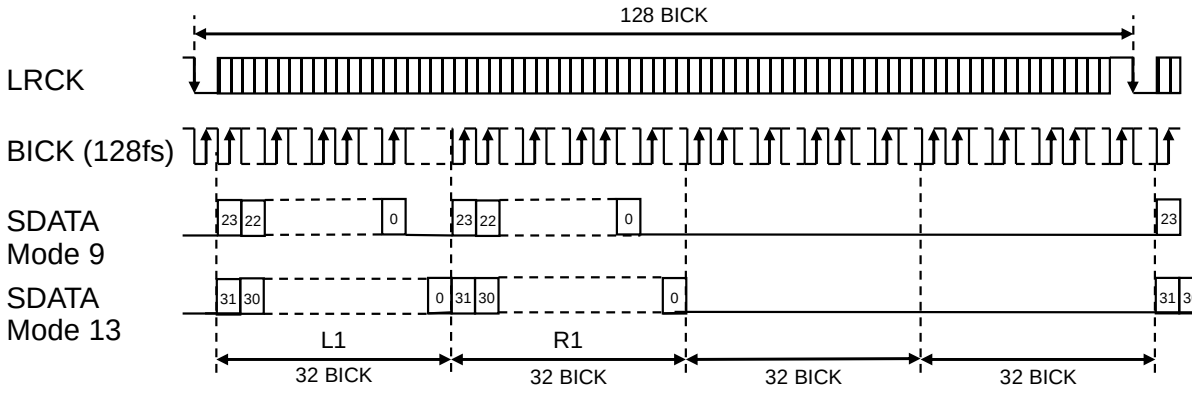


Figure 35. TDM128, 24-bit/32-bit I²S compatible (Mode 9/13) Timing

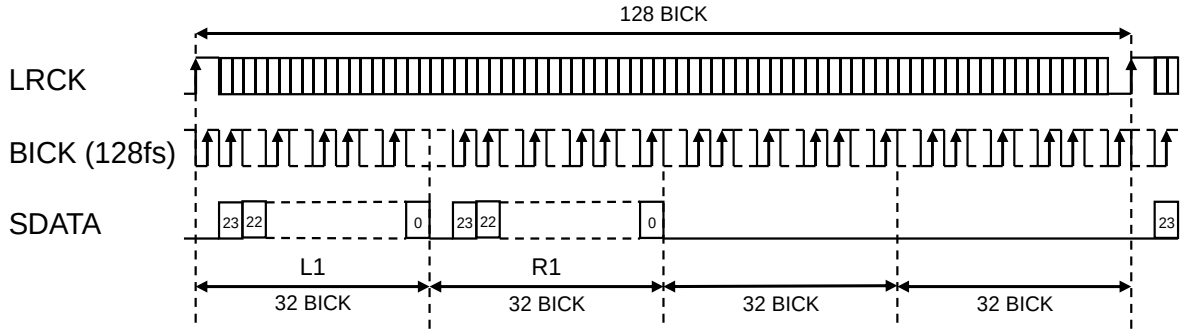


Figure 36. TDM128, 24-bit LSB justified (Mode 10) Timing

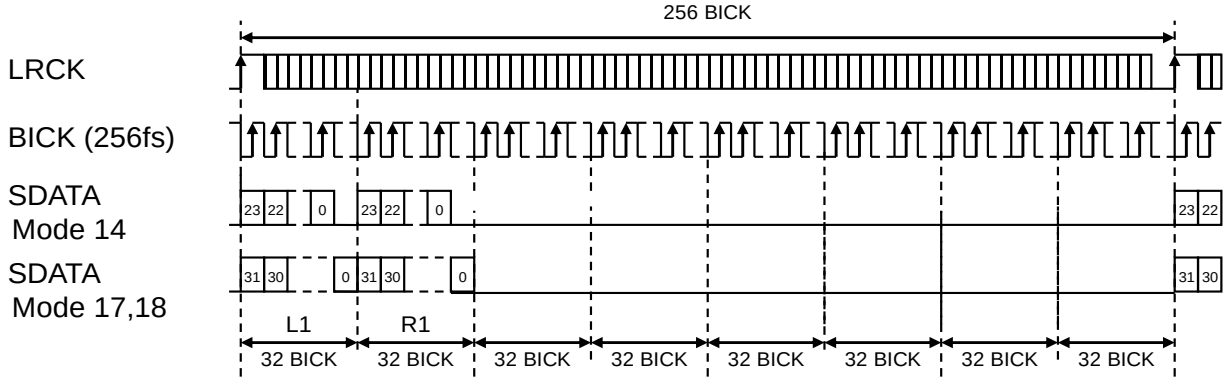


Figure 37. TDM256, 24-bit MSB justified, 32-bit MSB/LSB justified (Mode 14/17/18) Timing

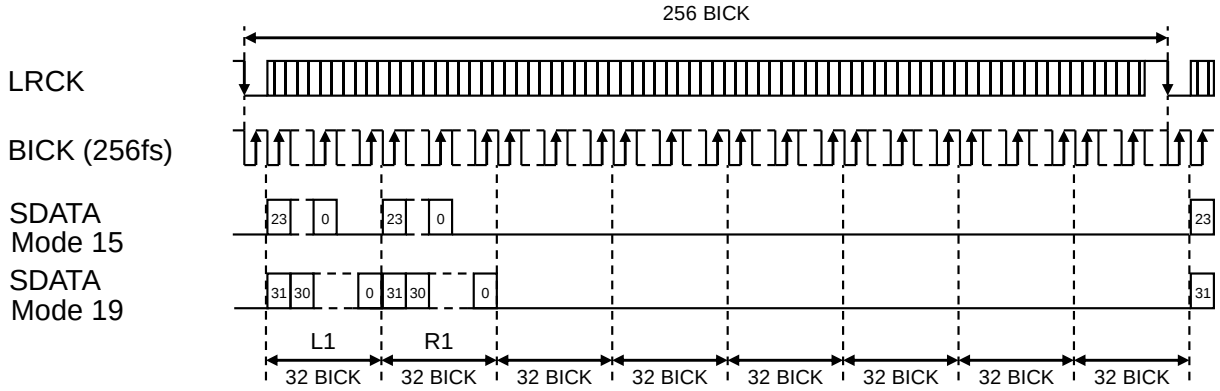


Figure 38. TDM256, 24-bit/32-bit I²S compatible (Mode 15/19) Timing

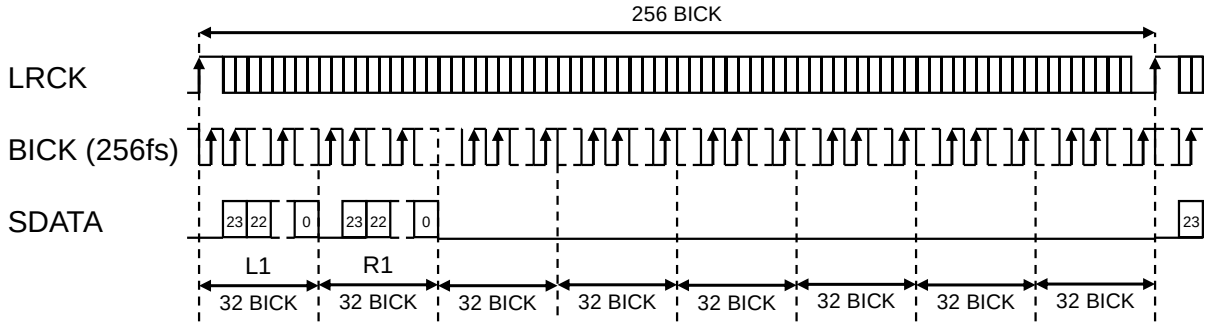


Figure 39. TDM256, 24-bit LSB justified (Mode 16) Timing

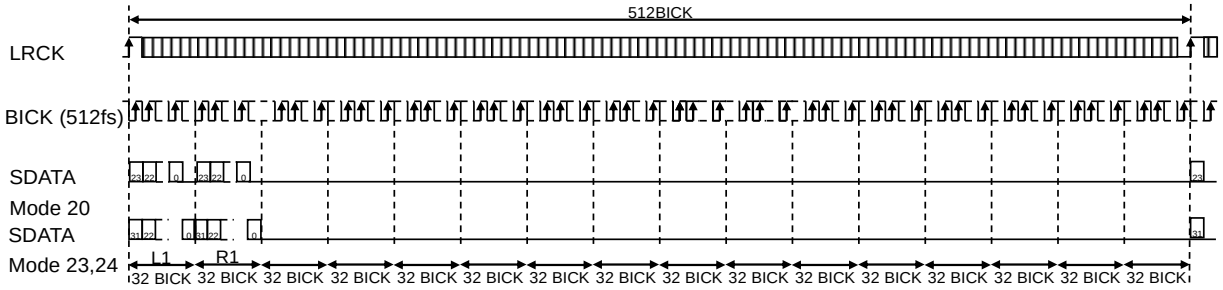


Figure 40. TDM512, 24-bit MSB justified, 32-bit LSB/MSB justified (Mode 20/23/24) Timing

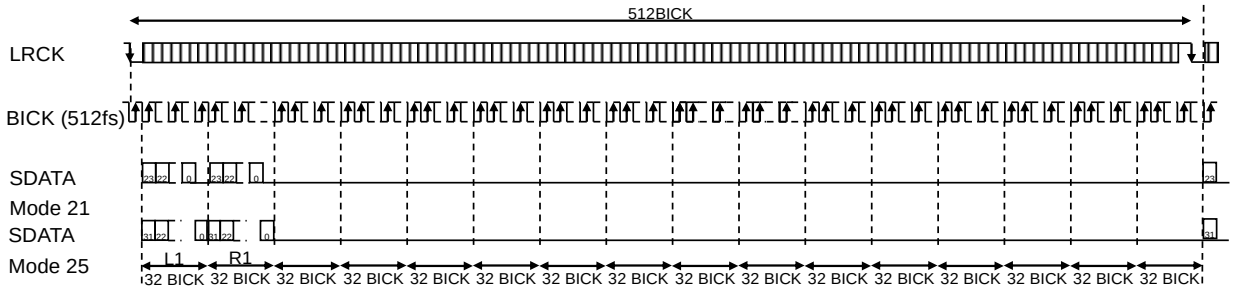


Figure 41. TDM512, 24-bit/32-bit I²S Compatible (Mode 21/25) Timing

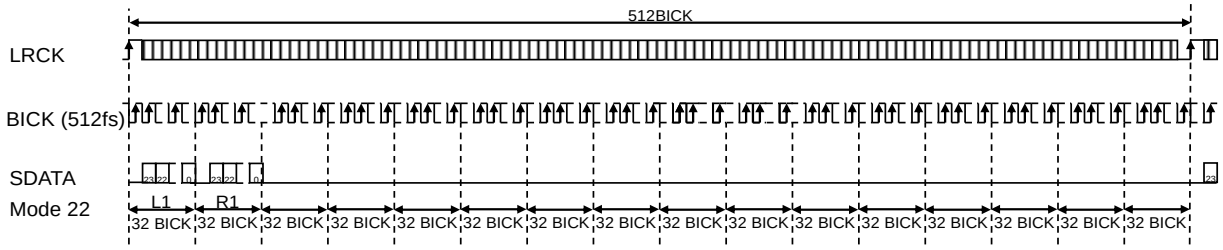


Figure 42. TDM512, 24-bit LSB justified (Mode 22) Timing

9.4.1.2. Data Slots

Data slots during one LRCK cycle are defined as Figure 43 – Figure 46. The slots for the two channels to be assigned can be selected using the SDS[2:0] bits as shown in Table 23. In Pin Control mode, the L1 and R1 slots are assigned.

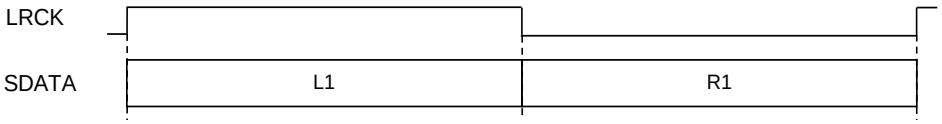


Figure 43. Data Slot in Normal mode

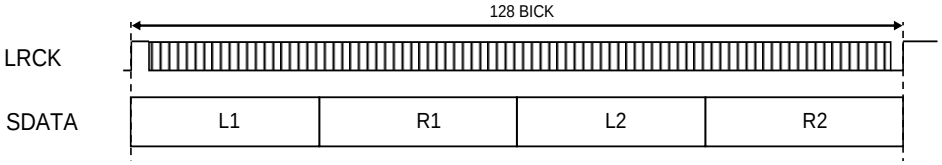


Figure 44. Data Slot in TDM128 mode

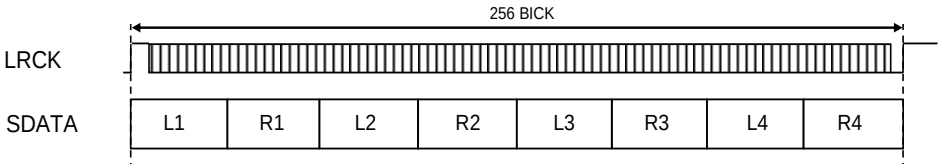


Figure 45. Data Slot in TDM256 mode

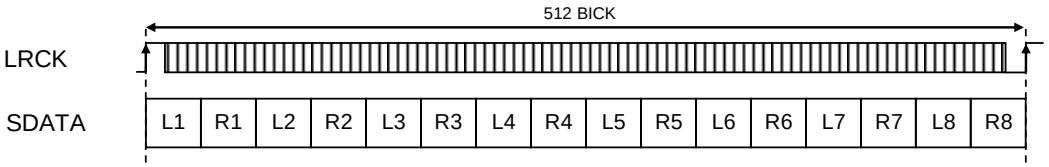


Figure 46. Data Slot in TDM512 mode

Table 23. Slot Select

Input Mode	SDS2 bit	SDS1 bit	SDS0 bit	Slot L-ch	Slot R-ch	
Normal	*	*	*	L1	R1	
TDM128	*	*	0	L1	R1	(default)
	*	*	1	L2	R2	
TDM256	*	0	0	L1	R1	(default)
	*	0	1	L2	R2	
	*	1	0	L3	R3	
	*	1	1	L4	R4	
TDM512	0	0	0	L1	R1	(default)
	0	0	1	L2	R2	
	0	1	0	L3	R3	
	0	1	1	L4	R4	
	1	0	0	L5	R5	
	1	0	1	L6	R6	
	1	1	0	L7	R7	
	1	1	1	L8	R8	

(*: Do not care)

9.4.1.3. Daisy Chain

The AK4497S supports cascading of multiple devices by daisy chain connection in TDM512/256 mode. DCHAIN bit or DCHAIN pin controls Daisy Chain mode (Table 24). SDS[2:0] bits setting will be invalid in Daisy Chain mode.

Table 24. Daisy Chain Control

DCHAIN bit / pin	Daisy Chain	TDMO pin Output	
0	Disable	L	(default)
1	Enable	Shifted SDATA	

- Daisy Chain in TDM512 mode

Figure 47 shows the daisy chain connections in TDM512 mode. 16-ch data is input to the SDATA pin of the top AK4497S (8th) and its TDMO pin is connected to the SDATA pin of the next AK4497S (7th). Up to eight AK4497S devices can be connected in this way.

Figure 48 shows the data input/output example of daisy chain in TDM512 mode. Each AK4497S outputs SDATA delayed by 2 slots to the TDMO pin. Each AK4497S uses the last 2 slots. Please note that the last 2 slots will be used even if less than eight AK4497S are daisy chained. The settings of DIF[2:0] bits of all AK4497S must be the same.

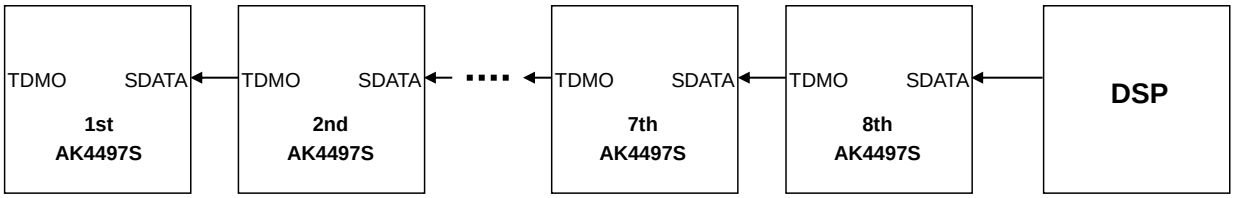


Figure 47. Daisy Chain (TDM512 mode)

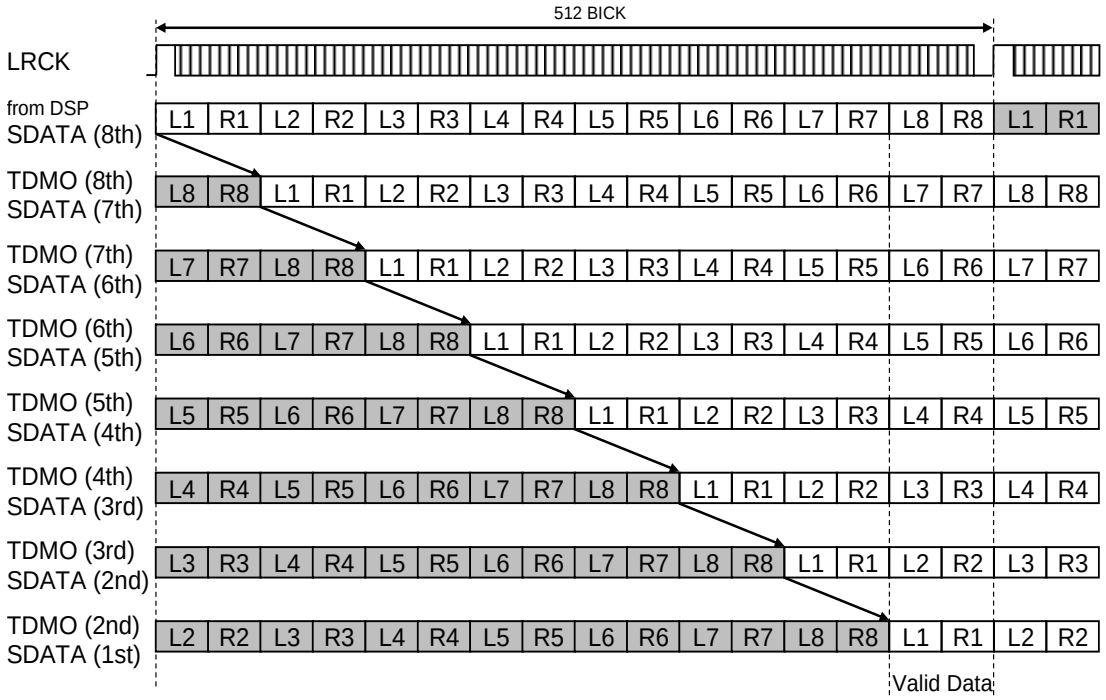


Figure 48. Daisy Chain (TDM512 mode)

・ Daisy Chain TDM256 mode

Figure 49 shows the daisy chain connections in TDM256 mode. 8-ch data is input to the SDATA pin of the top AK4497S (4th) and its TDMO pin is connected to the SDATA pin of the next AK4497S (3rd). Up to four AK4497S devices can be connected in this way.

Figure 50 shows the data input/output example of daisy chain in TDM256 mode. Each AK4497S outputs SDATA delayed by 2 slots to the TDMO pin. Each AK4497S uses the last 2 slots. Please note that the last 2 slots will be used even if less than four AK4497S are daisy chained. Settings of the DIF[2:0] bits of all AK4497S must be the same.

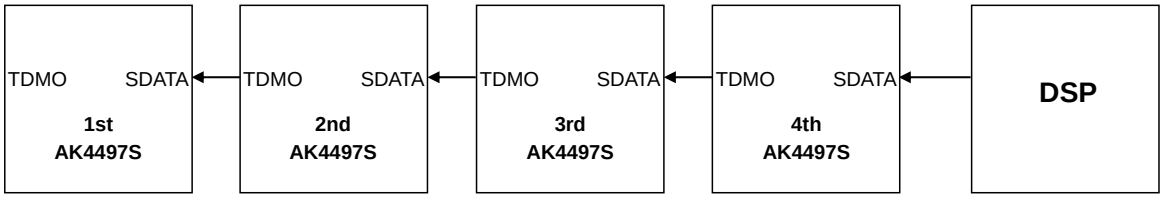


Figure 49. Daisy Chain (TDM256 mode)

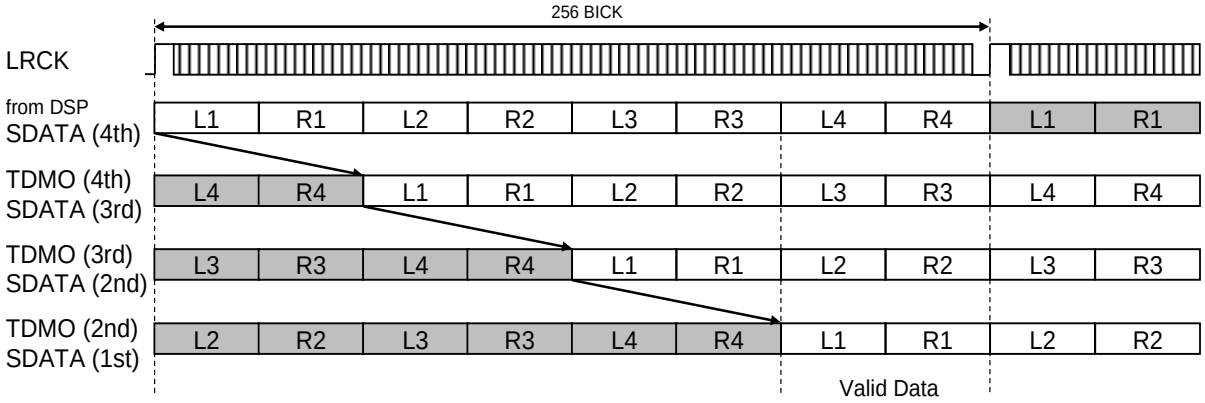


Figure 50. Daisy Chain (TDM256 mode)

9.4.2. DSD mode (Register Control mode only)

In DSD mode, L channel and R channel data must be input to the DSDL1, DSDR1 pins or the DSDL2, DSDR2 pins, respectively by synchronizing to DCLK. Input pins can be selected by the DSDPATH bit. When the DSDPATH bit = “0”, the DSDL2, DSDR2 pins are enabled. When the DSDPATH bit = “1”, the DSDL1, DSDR1 pins are enabled. In addition to normal mode DSD data, phase modulation mode DSD data can also be input without any settings. The polarity of DCLK can be selected by the DCKB bit.

In DSD mode, the settings of the DIF[2:0] bits are ignored. The frequency of DCLK is selected between 64fsb, 128fsb, 256fsb and 512fsb by the DSDSEL[1:0] bits. Phase modulation function is not available in 512fsb (DSDSEL[1:0] bits = “11”).

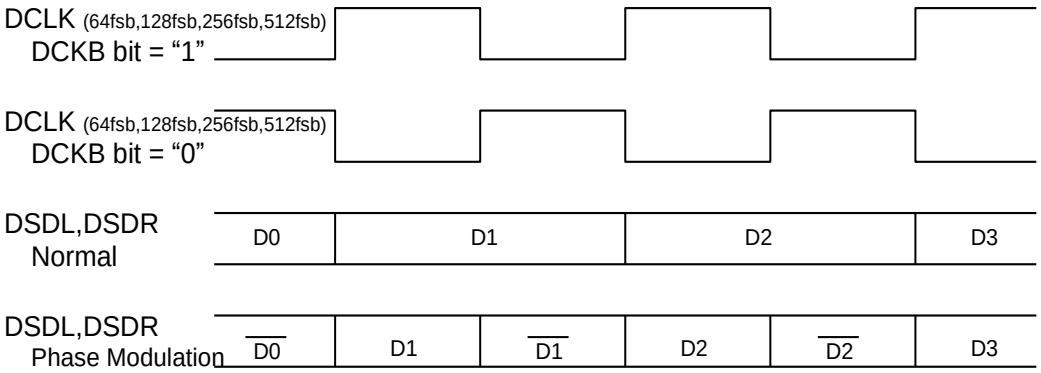


Figure 51. DSD mode Timing

9.4.3. External Digital Filter mode (EXDF mode)

The audio serial data is input to the DINL and DINR pins in synchronization with BCK and WCK. The audio serial data is latched on the rising edge of BCK. Three formats are available (Table 25) by the DIF[2:0] bits setting.

Table 25. Audio Serial Data Interface Format (EXDF mode)

Mode	DIF2 bit	DIF1 bit	DIF0 bit	Data Format	
0	0	0	0	16-bit LSB justified	
1	0	0	1	N/A	
2	0	1	0	16-bit LSB justified	
3	0	1	1	N/A	
4	1	0	0	24-bit LSB justified	
5	1	0	1	32-bit LSB justified	
6	1	1	0	24-bit LSB justified	(default)
7	1	1	1	32-bit LSB justified	

(N/A: Not available)

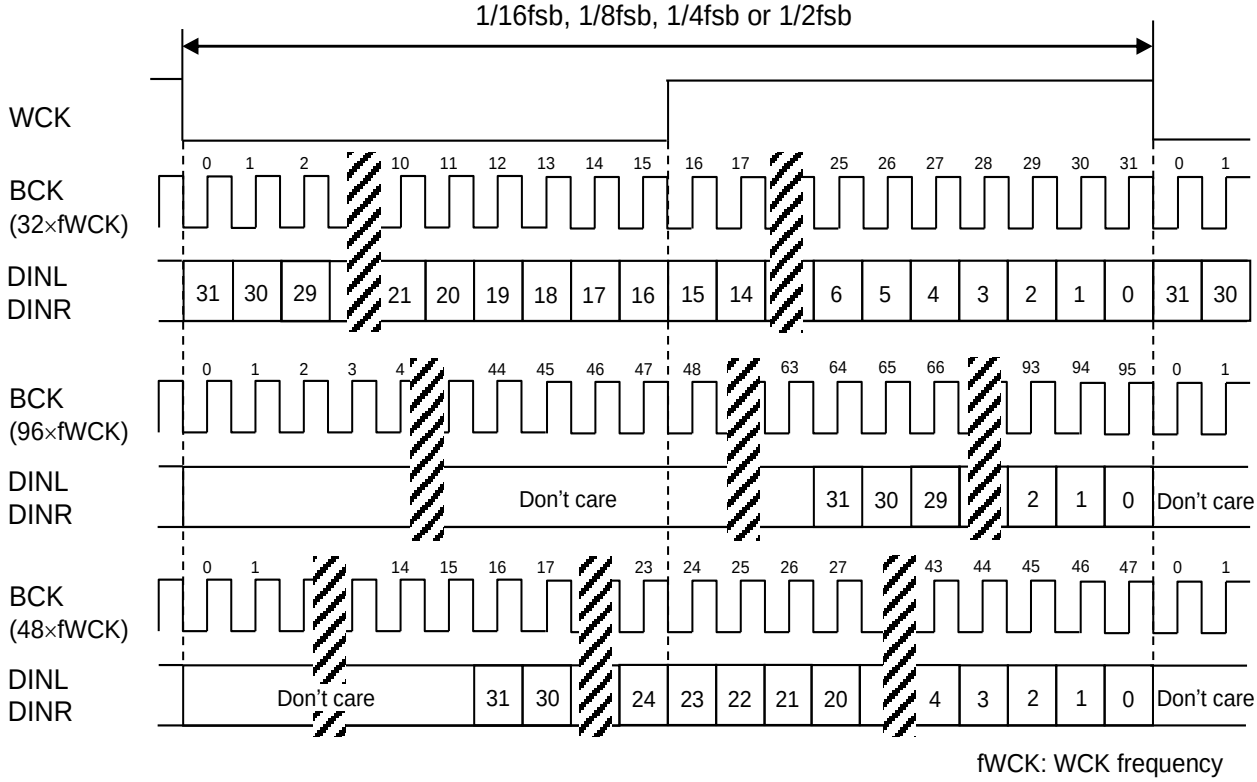


Figure 52. EXDF mode Timing Example (32-bit LSB justified)

9.5. Digital Filter

Six types of digital filter in PCM mode and two types of digital filter in DSD mode are available in the AK4497S for sound color selection of music playback.

9.5.1. PCM mode

The digital filter can be selected by the SD, SLOW and SSLOW pins in Pin Control mode or by the SD, SLOW and SSLOW bits in Register Control mode (Table 26).

Table 26. Digital Filter Setting in PCM mode

SSLOW bit / pin	SD bit / pin	SLOW bit / pin	Filter	
0	0	0	Sharp Roll-off Filter	
0	0	1	Slow Roll-off Filter	
0	1	0	Short Delay Sharp Roll-off Filter	(default)
0	1	1	Short Delay Slow Roll-off Filter	
1	0	0	Super Slow Roll-off Filter	
1	0	1	Super Slow Roll-off Filter	
1	1	0	Low Dispersion Short Delay Filter	
1	1	1	Programmable FIR Filter	

Note: The programmable FIR filter (SSLOW, SD, SLOW bits = “111”) is valid only in Register Control mode. The programmable FIR filter (SSLOW, SD, SLOW bits = “111”) is not active in Pin Control mode, and the output signal is muted.

9.5.2. DSD mode

The cutoff frequency of digital filter can be switched by the DSDF bit. Table 27 shows the cutoff frequency at fsb = 44.1 kHz. The cutoff frequency tracks the base sampling frequency (fsb).

Table 27. DSD Filter Select

DSDF bit	Cut Off Frequency @fsb = 44.1 kHz				
	DSD64	DSD128	DSD256	DSD512	
0	39 kHz	78 kHz	156 kHz	312 kHz	(default)
1	76 kHz	152 kHz	304 kHz	608 kHz	

9.6. Programmable FIR Filter (PCM mode)

The AK4497S has a programmable 24-bit FIR filter. Filter coefficients of maximum 209 taps can be set up to the 1st stage, 4x over sampling, zero padded FIR filter when the SSLOW, SLOW, SD bits = “111”. The programmable filter is valid only in Register Control mode (PSN pin = “L”).

There is coefficient RAM (CRAM), which stores the filter coefficient. By setting CRAMW bit = “1”, the filter coefficients stored in CRAM can be changed.
The filter coefficients can be changed by writing addresses 0EH to 11H. Follow steps 1 through 3 below. It can be written when the STBYN bit = “0”, RSTN bit = “0”. MCLK, BICK and LRCK should be input.

Step 1. Write the CRAMW bit (0DH) = “1”, CRAMR bit (0DH) = “0”

Step 2. Specify the tap address by setting register addrss 0EH. Write a value within the range of 1~209 to the FIRT[7:0] bits in unsigned binary code. The FIRT[7] bit will be the MSB and the FIRT[0] bit will be the LSB. Coefficient write is not executed when writing a tap address other than 1 ~ 209.

Step 3. Write 24-bit signed binary code filter coefficients (FIRC[23:0] bits) as follows:
Step 3a. Write MSB byte data FIRC[23:16] bits (address 0FH).

Step 3b. Write middle byte data FIRC[15:8] bits (address 10H).
Step 3c. Write LSB byte data FIRC[7:0] bits (address 11H).

After completion of writing to 11H in step 3c, the filter coefficients of 0FH, 10H, and 11H are applied to the tap specified by 0EH. If steps 1 through 3 are not followed, the coefficients may not be written correctly, and the expected filter processing may not be performed.

Repeat steps 1 through 3 for each filter tap up to 209 taps maximum.

Write coefficient "000000H" from the first unused tap address to the last tap address 209 when the number of taps is under 209.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0EH	FIR tap address	FIRT7	FIRT6	FIRT5	FIRT4	FIRT3	FIRT2	FIRT1	FIRT0
0FH	FIRC[23:16]	FIRC23	FIRC22	FIRC21	FIRC20	FIRC19	FIRC18	FIRC17	FIRC16
10H	FIRC[15:8]	FIRC15	FIRC14	FIRC13	FIRC12	FIRC11	FIRC10	FIRC09	FIRC08
11H	FIRC[7:0]	FIRC07	FIRC06	FIRC05	FIRC04	FIRC03	FIRC02	FIRC01	FIRC00

The default value of the programmable filter coefficient is all zero. When any filter other than the programmable filter is selected after changing the filter coefficient its value will be kept. To initialize the filter coefficients stored in CRAM to those of the default value, write the CRAMCLR bit = "1". It can be written even when the STBYN bit = "0" and RSTN bit = "0". MCLK, BICK and LRCK should be input.

When changing the filter coefficient, the output volume should be muted by the volume control or soft mute function until all coefficient writings are completed. If not, click noise may occur when writing coefficients. DC gain of the filter should be set not higher than 0 dB. However, passband ripple is accepted up to +0.1 dB. To obtain 0 dB filter DC gain, set the filter coefficient so that the sum of coefficient becomes $4*(2^{23}-1) = 33554428$. Absolute value summation of the filter coefficient must satisfy following four conditions.

$$\sum_{n=1}^{53} |h(4n-3)| = |h(1)| + |h(5)| + \cdots + |h(201)| + |h(205)| + |h(209)| < 33554428$$

$$\sum_{n=1}^{52} |h(4n-2)| = |h(2)| + |h(6)| + \cdots + |h(202)| + |h(206)| < 33554428$$

$$\sum_{n=1}^{52} h(4n-1)| = |h(3)| + |h(7)| + \cdots + |h(203)| + |h(207)| < 33554428$$

$$\sum_{n=1}^{52} |h(4n)| \quad = |h(4)| + |h(8)| + \cdots + |h(204)| + |h(208)| < 33554428$$

The coefficients set at the tap addresses specified by 0DH and 0EH can be read at addresses 12H, 13H and 14H. Follow steps 1 – 3 below.

Step 1. Write the CRAMR bit (0DH) = "1" and CRAMW bit (0DH) = "0".
Step 2. Specify the tap address by the FIRT[7:0] bits.
Step 3a – 3b. Read RFIRC[23:16] bits, read RFIRC[15:8] bits, read RFIRC[7:0] bits (assemble as RFIRC[23:0] bits).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
12H	RFIRC[23:16]	RFIRC23	RFIRC22	RFIRC21	RFIRC20	RFIRC19	RFIRC18	RFIRC17	RFIRC16
13H	RFIRC[15:8]	RFIRC15	RFIRC14	RFIRC13	RFIRC12	RFIRC11	RFIRC10	RFIRC09	RFIRC08
14H	RFIRC[7:0]	RFIRC07	RFIRC06	RFIRC05	RFIRC04	RFIRC03	RFIRC02	RFIRC01	RFIRC00

9.7. De-emphasis Filter (PCM mode)

A digital de-emphasis filter (tc = 50/15 μs) is available for 32 kHz, 44.1 kHz, or 48 kHz sampling rates in Register Control mode, and for 44.1 kHz sampling rate only in Pin Control mode. The de-emphasis filter is enabled or disabled by the DEM[1:0] bits or DEM0 pin according to the control mode. The DEM[1:0] bits are ignored in DSD and EXDF modes. The DEM[1:0] setting value is held even if the D/A Conversion Mode is switched among PCM, DSD and EXDF modes.

Table 28. De-emphasis Control (Register Control mode)

DEM1 bit	DEM0 bit	fs Mode	
0	0	44.1 kHz	
0	1	OFF	(default)
1	0	48 kHz	
1	1	32 kHz	

Table 29. De-emphasis Control (Pin Control mode)

DEM0 pin	fs Mode
L	44.1 kHz
H	OFF

9.8. Digital Attenuator (PCM, DSD and EXDF mode; Register Control mode only)

The AK4497S has channel independent digital attenuators. Attenuation level range is from 0 dB to −127 dB in 0.5 dB steps, also mute. The attenuation level when the ATTL/R[7:0] bits are FFH is defined as 0 dB. When changing the attenuation level, it is executed in soft transition, thus no switching noise occurs during these transitions.

Table 30. Attenuation Level of Digital Attenuator

ATTL/R[7:0] bits	Attenuation Level	
FFH	+0 dB	(default)
FEH	−0.5 dB	
FDH	−1.0 dB	
:	:	
:	:	
02H	−126.5 dB	
01H	−127.0 dB	
00H	MUTE (−∞ dB)	

The soft transition speed of attenuation level is set by the ATS[1:0] bits (Table 31). Register values of attenuation settings will be kept even if switching the PCM/EXDF and DSD modes.

Table 31. Transition Time (0 dB to MUTE)

Mode	ATS1 bit	ATS0 bit	Transition Time			
			PCM mode	EXDF mode	DSD mode	
0	0	0	4080/fs	4080*WCK cycle	4080/(2 x fsb)	(default)
1	0	1	2040/fs	2040*WCK cycle	2040/(2 x fsb)	
2	1	0	510/fs	510*WCK cycle	510/(2 x fsb)	
3	1	1	255/fs	255*WCK cycle	255/(2 x fsb)	

It takes 4080/fs (92.5 ms @ fs = 44.1 kHz) from “FFH” (0 dB) to “00H” (MUTE) when the ATS[1:0] bits = "00" in PCM mode.

If the ATTL/R[7:0] bits setting is changed during reset state, the digital attenuator will become the setting value after releasing reset. It will change to the setting value immediately if the ATTL/R[7:0] bits setting is changed within 10/fsb after releasing reset.

9.9. Volume Bypass (DSD mode; Register Control mode only)

The AK4497S has Volume Bypass function for playing back a DSD signal. This mode is selectable by the DSDD bit (Table 32). When setting the DSDD bit = "1", the output volume control and zero detect functions are not available.

Table 32. DSD Playback Path Select

DSDD bit	Playback Path	
0	Normal Path	(default)
1	Volume Bypass	

9.10. Gain Adjustment Function (PCM mode, DSD mode, EXDF mode)

The AK4497S has a gain adjustment function. The analog output amplitude can be adjusted by the GC[2:0] bits in Register Control mode or by the GAIN pin in Pin Control mode. If there is no attenuation by an external digital filter, the output level in EXDF mode will be the same as in PCM mode.

Table 33. Output Level Selection

GC2 bit	GC1 bit	GC0 bit	AOUTLP/N, AOUTRP/N Output Level			
			PCM	DSD Normal Path	DSD Volume Bypass	
0	0	0	2.8 Vpp	2.8 Vpp	2.5 Vpp	(default)
0	0	1	2.8 Vpp	2.5 Vpp	2.5 Vpp	
0	1	0	2.5 Vpp	2.5 Vpp	2.5 Vpp	
0	1	1	2.5 Vpp	2.5 Vpp	2.5 Vpp	
1	0	0	3.75 Vpp	3.75 Vpp	2.5 Vpp	
1	0	1	3.75 Vpp	2.5 Vpp	2.5 Vpp	
1	1	0	2.5 Vpp	2.5 Vpp	2.5 Vpp	
1	1	1	2.5 Vpp	2.5 Vpp	2.5 Vpp	

Table 34. Output Level Selection (Valid Only in PCM mode)

GAIN pin	AOUTLP/LN/RP/RN Output Level
L	2.8 Vpp
H	3.75 Vpp

Note 50. The DSDF bit must be set to "0" if the GC[2:0] bits are set to "100" when using DSD normal path. Click noise may occur if the DSDF bit is set to "1".

9.11. Zero Detection (PCM mode, DSD mode, EXDF mode)

AK4497S has a zero detection function for each channel. When the input data at each channel is continuously zeros for 8192/fsb, the DZFL/R pin outputs zero detection flag. In DSD512 mode, the zero detection flag is set for zeros 16384/fsb.

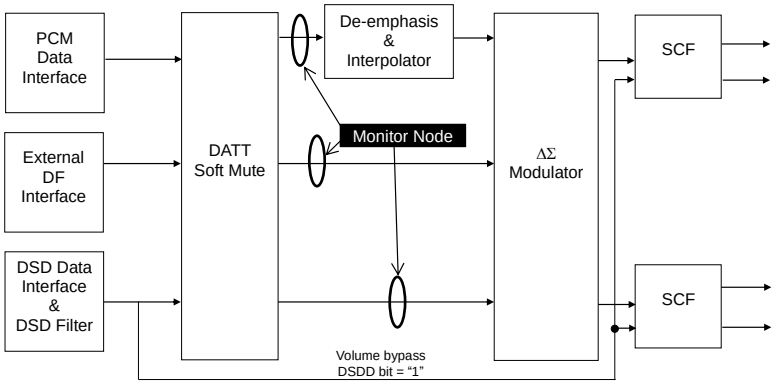


Figure 53. Zero Detection Monitor Node

When zero is detected, the DZFL/R pins become “H”. After zero detection, if data other than zero is input, the DZFL/R pin immediately returns to “L”. If the RSTN bit is set to “0”, the DZFL/R pins of both go to “H”. After returning the RSTN bit to “1”, the DZFL/R pin returns to “L” 4/fsb after any data bit of “1” is input.

If the DZFM bit is set to “1”, the DZFL/R pins of both go to “H” only when both channels detect zeros. The zero detection can be disabled by setting the DZFE bit to “0”. In this case, the DZFL/R pins are always “L”. Zero detection is also disabled when Volume Bypass is selected in DSD mode (Table 32). Polarity of the zero detection flag on the DZFL/R pins can be inverted by the DZFB bit.

Table 35. Zero Detection (DZFB bit = “0”)

DZFE bit	RSTN bit	DZFM bit	L channel	R channel	DZFL pin	DZFR pin
0	-	-	-	-	L	L
1	0	-	-	-	H	H
	1	0	Not Zero	Not Zero	L	L
			Not Zero	Zero	L	H
			Zero	Not Zero	H	L
			Zero	Zero	H	H
		1	Not Zero	Not Zero	L	L
			Not Zero	Zero	L	L
			Zero	Not Zero	L	L
			Zero	Zero	H	H

9.12. L/R Channel Output Signal Select, Phase Inversion Function (PCM mode, DSD mode, EXDF mode)

In Register Control mode, the input and output combination of the AK4497S can be changed by the MONO and SELLR bits. In addition, the output signal phase can be inverted by the INVL and INVR bits. These functions are available on all conversion modes. In Pin Control mode, the phase of R channel output can be inverted by setting the INVR pin.

Table 36. Channel Select and Phase Inversion (Register Control mode)

MONO bit	SELLR bit	INVL bit	INVR bit	L-ch Data	R-ch Data
0	0	0	0	L-ch In	R-ch In
		0	1	L-ch In	R-ch In Invert
		1	0	L-ch In Invert	R-ch In
		1	1	L-ch In Invert	R-ch In Invert
0	1	0	0	R-ch In	L-ch In
		0	1	R-ch In	L-ch In Invert
		1	0	R-ch In Invert	L-ch In
		1	1	R-ch In Invert	L-ch In Invert
1	0	0	0	L-ch In	L-ch In
		0	1	L-ch In	L-ch In Invert
		1	0	L-ch In Invert	L-ch In
		1	1	L-ch In Invert	L-ch In Invert
1	1	0	0	R-ch In	R-ch In
		0	1	R-ch In	R-ch In Invert
		1	0	R-ch In Invert	R-ch In
		1	1	R-ch In Invert	R-ch In Invert

Table 37. Phase Inversion (Pin Control mode)

INVR pin	L-ch Data	R-ch Data
0	L-ch In	R-ch In
1	L-ch In	R-ch In Invert

9.13. Sound Quality (PCM mode, DSD mode, EXDF mode)

Sound quality of the AK4497S can be controlled by setting the SC[2:0] bits. The Analog Characteristics are specified and only guaranteed in Setting 1 and Setting 3 combined.

Table 38. Sound Quality Mode Select

SC1 bit	SC0 bit	Sound	
0	*	Analog internal current, maximum (Setting 1)	(default)
1	*	Analog internal current, medium (Setting 2)	

(*: Don’t care)

Table 39. Sound Quality Mode Select

SC2 bit	Sound	
0	Measurement mode (Setting 3)	(default)
1	Sound Quality mode (Setting 4)	

9.14. DSD Signal Full Scale Detection

The AK4497S has full-scale detection function for each channel in DSD mode. Figure 54 shows a block diagram of DSD signal playback. Full-scale detection does not work in PCM mode and EXDF mode.

9.14.1. Full-scale Detection

The DSD full-scale detection block receives input data of the DSDL pin and DSDR pin via the DSD Data Interface block. The full-scale detection flag (DML, DMR) for corresponding channel becomes “1” when the DSDL pin or DSDR pin input data is continuously “0” (−Full scale) or “1” (+Full scale) for detection time. The detection time is set by the DDMT[1:0] bits as shown in Table 40. The DML and DMR flags can be read out at the register. These bits only indicate “1” while full-scale data is input. Full-scale detection signal can also be output from the DZFL pin or DZFR pin by setting the DDMOE bit = “1”. Refer to Table 41 for details.

Table 40. DSD Signal Full-scale Detection Time Setting

DDMT1 bit	DDMT0 bit	Detection Time	Register Delay	
0	0	256 DCLK Cycles	264 DCLK Cycles	(default)
0	1	512 DCLK Cycles	520 DCLK Cycles	
1	0	1024 DCLK Cycles	1032 DCLK Cycles	
1	1	128 DCLK Cycles	136 DCLK Cycles	

Table 41. Output Signal of the DZFL/DZFR pins (DDMOE bit = “1”)

DZFE bit	DZFM bit	DZFL pin	DZFR pin
*	0	DML L-ch Full-Scale Detection Flag	DMR R-ch Full-Scale Detection Flag
0	1	L	OR Signal of DML and DMR
1		AND Signal of L-ch and R-ch Zero Detection Flags	

(*: Do not care)

9.14.2. Mute Function with Full-scale Detection

When the DDM bit = “1”, if either the L channel or R channel full scale flag becomes “1”, the DSD filter output is fixed to zero data. As a result, the analog outputs of both channels are muted. At the same time, the DATT attenuation level becomes muted (−∞ dB). To prevent click noise, the DSD Data Interface block output signal is delayed by the detection time + 8DCLK cycles by register block until the signal is muted completely (Table 40). The analog output delay also increases accordingly.

9.14.3. Recovery from Full-scale Detection

Full-scale detection state is released when the input DSD data is toggled (Table 42). When the DSDD bit = “1” (Volume Bypass), normal operation returns immediately after the full-scale detection state is released. When the DSDD bit = “0” (Normal Path), normal operation returns immediately, and the analog output returns to the set level with soft transition. The transition time follows the ATS[1:0] bits settings.

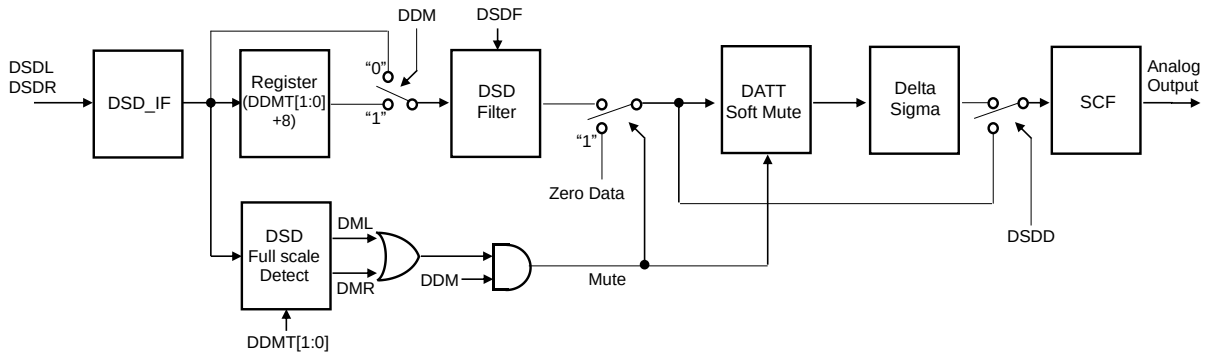
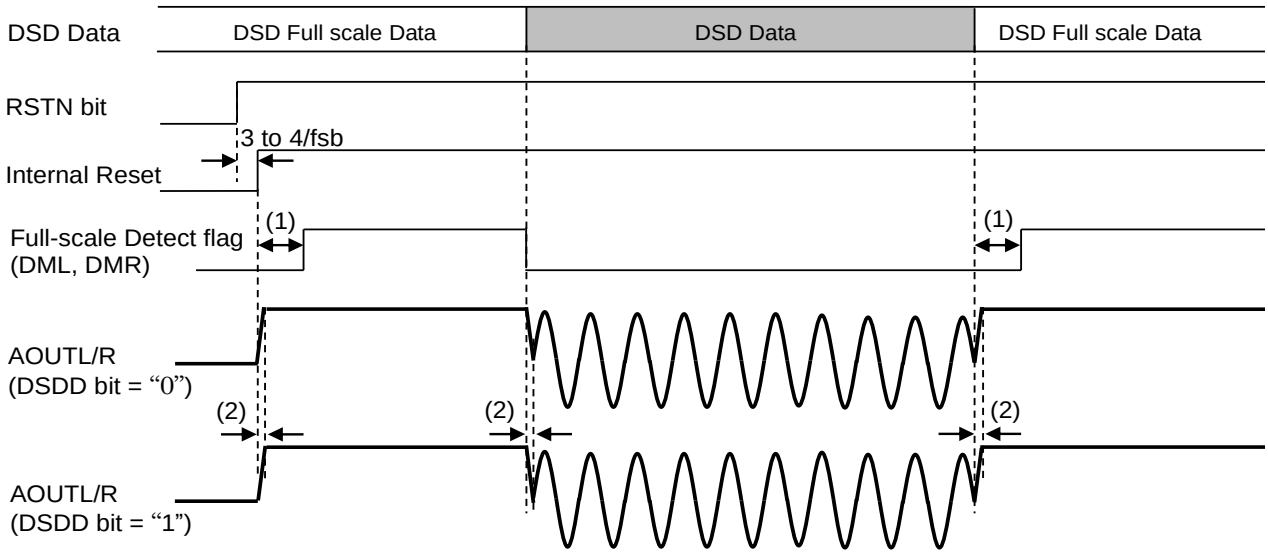


Figure 54. DSD Block Diagram

The full-scale detection function assumes full-scale input that may occur when switching from PCM mode or EXDF mode to DSD mode. It prevents click noise when the input signal transitions from zero data to full-scale or from full-scale to zero data. However, click noise may occur when switching from signaled state to full-scale or from full-scale to signaled state.

Table 42. Mute Transition Time (DDM bit = "1")

DSDD bit	Mode	Mute Transition time	Mute Release time	
0	Normal Path	Rapidly	According to ATS[1:0] bits	(default)
1	Volume Bypass	Rapidly		

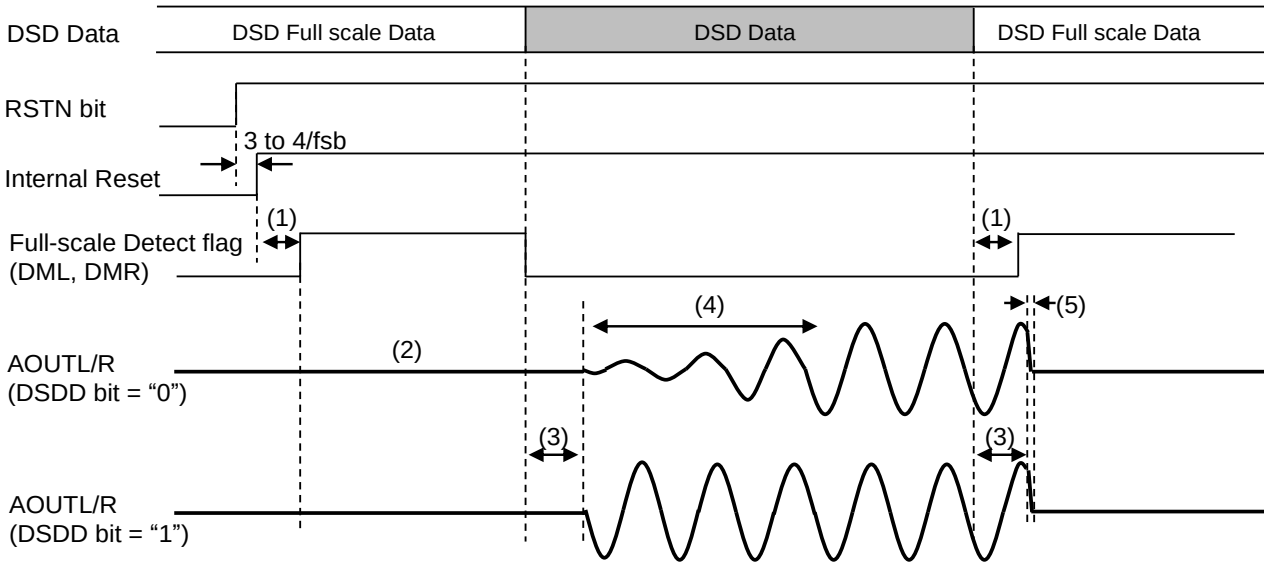


Note:

(1) Internal reset is released after 3/fsb to 4/fsb by setting the RSTN bit = "1". The full-scale detection flags become "1" if full-scale data is input for a period set by the DDMT[1:0] bits after releasing the internal reset. Excessive signals will be output from the analog output if the DSD input data is full-scale.

(2) The time it takes for the analog output to reach full scale depends on the cutoff frequency of the DSD filter, which is set by the DSDF bit.

Figure 55. Analog Output Waveform with DSD Full-scale Input (DDM bit = "0")



Notes:

(1) The internal reset is released after 3/fsb to 4/fsb by setting the RSTN bit = "1". The internal detection flag becomes "1" if the input data is full-scale for a period set by the DDMT[1:0] bits after releasing the internal reset.
(2) The analog output is forced to zero (VCML/R level) when the AK4497S detects full-scale data.
(3) The analog output delays for the period set by the DDMT[1:0] bits + 8DCLK cycles when the DDM bit = "1".
(4) The time to return to normal output state from full-scale state is controlled by transition time setting of the internal DATT circuit by ATS[1:0] bits.
(5) The analog output is forced to zero (VCML/R level) immediately when it becomes full-scale state during data input.

Figure 56. Analog Output Waveform with DSD Full-scale Input (DDM bit = "1")

9.15. Automatic D/A Conversion Mode Switching Function (PCM / EXDF mode ⇔ DSD mode; Register Control mode only)

The AK4497S has an automatic D/A conversion mode switching function that determines the PCM/DSD D/A conversion mode from the input clocks and data. This function is available by setting the ADPE bit = "1" when the PDN pin = "H" in register control mode. The DP bit is for manual setting. It will be ignored when the ADPE bit is "1".

The automatic D/A conversion mode switching function is valid between PCM mode and DSD mode or EXDF mode and DSD mode. PCM/DSD automatic switching is enabled by setting the ADPE bit = "1" when the EXDF bit = "0". EXDF/DSD automatic switching is enabled by setting the ADPE bit = "1" when the EXDF bit = "1". The EXDF bit setting should be made before changing the ADPE bit = "0" → "1". Note that automatic D/A conversion mode switching function is not available between PCM mode and EXDF mode.

The result of automatic mode detection can be read back by the ADP bit. When the ADPE bit = "1", the ADP bit outputs "0" if the detection result is PCM or EXDF mode and outputs "1" if it is DSD mode. This readback function of the ADP bit is invalid and "0" data is readout when the ADPE bit = "0".

When using the automatic D/A conversion mode switching function, the DSD full-scale detection mute function must be enabled (DDM bit = "1"). The DDM bit must be set while the STBYN bit or RSTN bit = "0". By setting the DDM bit = "1", the group delay will be 18/fsb longer in PCM/EXDF mode and 160 to 288 DCLK cycles longer according to full-scale detection time setting by the DDMT bit in DSD mode (Table 40). This function does not support DSD phase modulation format and the edge inversion function of DSD input data (DCKB bit = "1").

The automatic D/A conversion mode switching function supports both DSD data paths set by the DSDPATH bit.

9.15.1. Automatic D/A Conversion Mode Switching when the DSDPATH bit = "0"

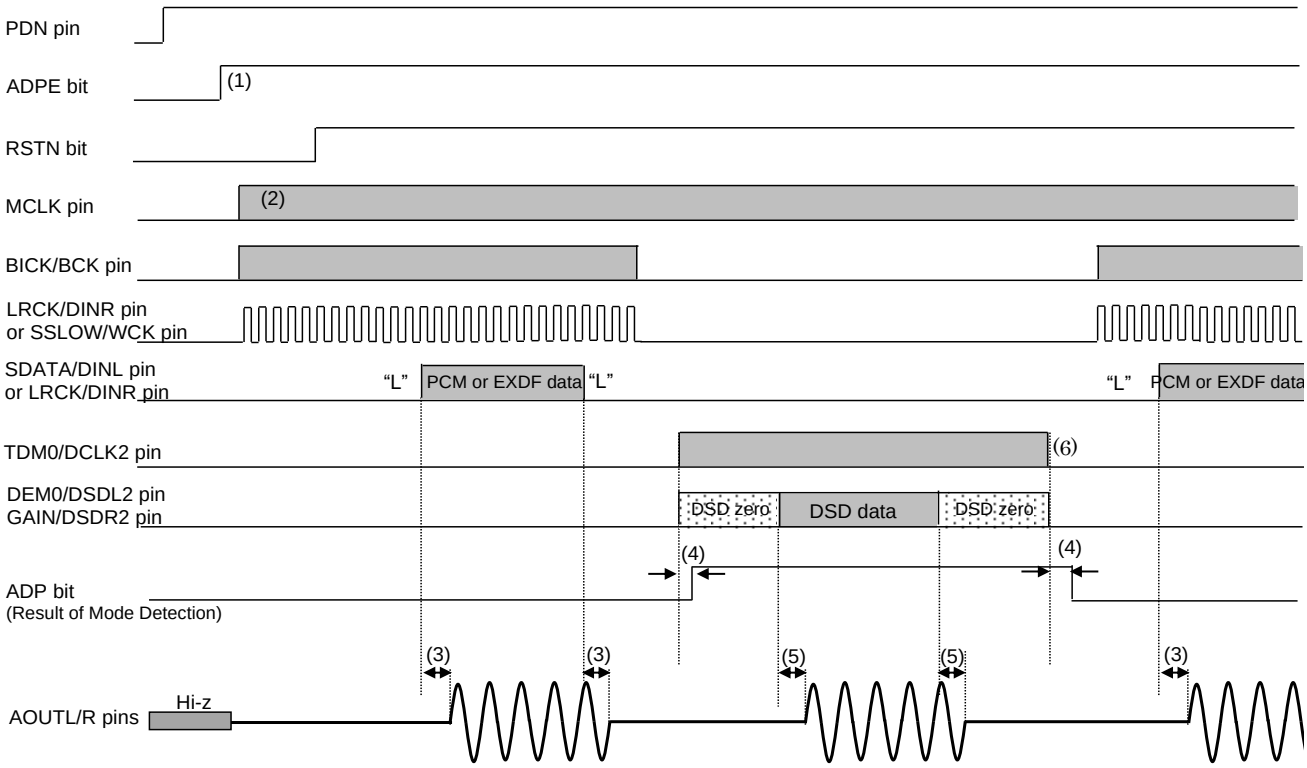
When the DSDPATH bit = "0", the AK4497S detects PCM (or EXDF) mode or DSD mode by counting a clock input to the TDM0/DCLK2 pin. MCLK should be input during mode detection.

The mode detection condition varies according to the DSDSEL[1:0] bits setting. The AK4497S detects DSD mode if the number of clock pulses in 1/fsb is in a range shown in Table 43, and PCM (or EXDF) mode is detected if not.

Table 43. Mode Detection Condition when DSDPATH = "0"

DSD Mode	DSDSEL[1:0] bits	Number of TDM0/DCLK2 Pulse in 1/fsb	Detection Result
DSD64	00	53 < pulse number < 77	DSD Mode
DSD128	01	106 < pulse number < 154	
DSD256	10	212 < pulse number < 308	
DSD512	11	424 < pulse number < 616	

When the mode is changed from PCM (or EXDF) to DSD, zero pattern data should be input to both L and R channels in DSD mode after inputting zero data to both channels in PCM (or EXDF) mode. When the mode is changed from DSD mode to PCM (or EXDF), zero pattern data should be input to both L and R channels in DSD mode before inputting zero data to both channels in PCM (or EXDF) mode. In this case, 1024/fsb of zero data input period is necessary. Refer to Figure 57 for the operation sequence.



Notes:

(1) Automatic mode switching between PCM (or EXDF) and DSD modes is enabled by setting the ADPE bit = "1".

(2) When the DSDPATH bit = "0", MCLK input is necessary for mode detection.

(3) In PCM mode, the analog output delay time becomes longer for about 18/fsb compared to when setting the ADPE bit = "0".

(4) The AK4497S transitions to DSD mode if the number of TDM0/DCLK2 input clock pulse in 1/fsb satisfies the condition. The condition of DSD mode detection is set by the DSDSEL[1:0] bits (Table 43).

(5) In DSD mode, the analog output delay time becomes longer compared to when setting the ADPE bit = "0". In this case, the delay time depends on the DDMT bit setting.

(6) The AK4497S transitions to PCM (or EXDF) mode if the number of DCLK input clock pulses does not satisfy the condition.

Figure 57. Mode Switching Sequence when DSDPATH bit = "0"

9.15.2. Automatic D/A Conversion Mode Switching when the DSDPATH bit = “1”

When the DSDPATH bit = “1”, the AK4497S detects PCM (or EXDF) mode or DSD mode from clock and data inputs of the BICK/BCK/DCLK1 pin, LRCK/DINR/DSDR1 pin and SSLOW/WCK pin.

9.15.2.1. Mode Detection Start Condition

If one of the five conditions shown below is satisfied, the AK4497S executes mode detection. The AK4497S keeps its previous mode instead of executing mode detection if any condition is not satisfied. These start conditions of mode detection are common regardless of the EXDF bit setting.

1. Input data of all channels are zero for a period set by the ADPT[1:0] bits (Table 44).
2. Downstream data of all channels are zero for a period set by the ADPT[1:0] bits (Table 44) because of the attenuation setting or SMUTE bit setting.
3. Input data of all channels are full-scale for a period set by the DDMT[1:0] bits in DSD mode (Table 40).
4. The STBYN bit = “0”
5. The RSTN bit = “0”

Table 44. Time until Mode Detection after Input Data becomes Zero

ADPT[1:0] bits	Wait Time	
00	8192/fsb + 18/fsb	(default)
01	4096/fsb + 18/fsb	
10	2048/fsb + 18/fsb	
11	1024/fsb + 18/fsb	

9.15.2.2. Mode Detection

- PCM/DSD Mode Automatic Switching (EXDF bit = “0”)

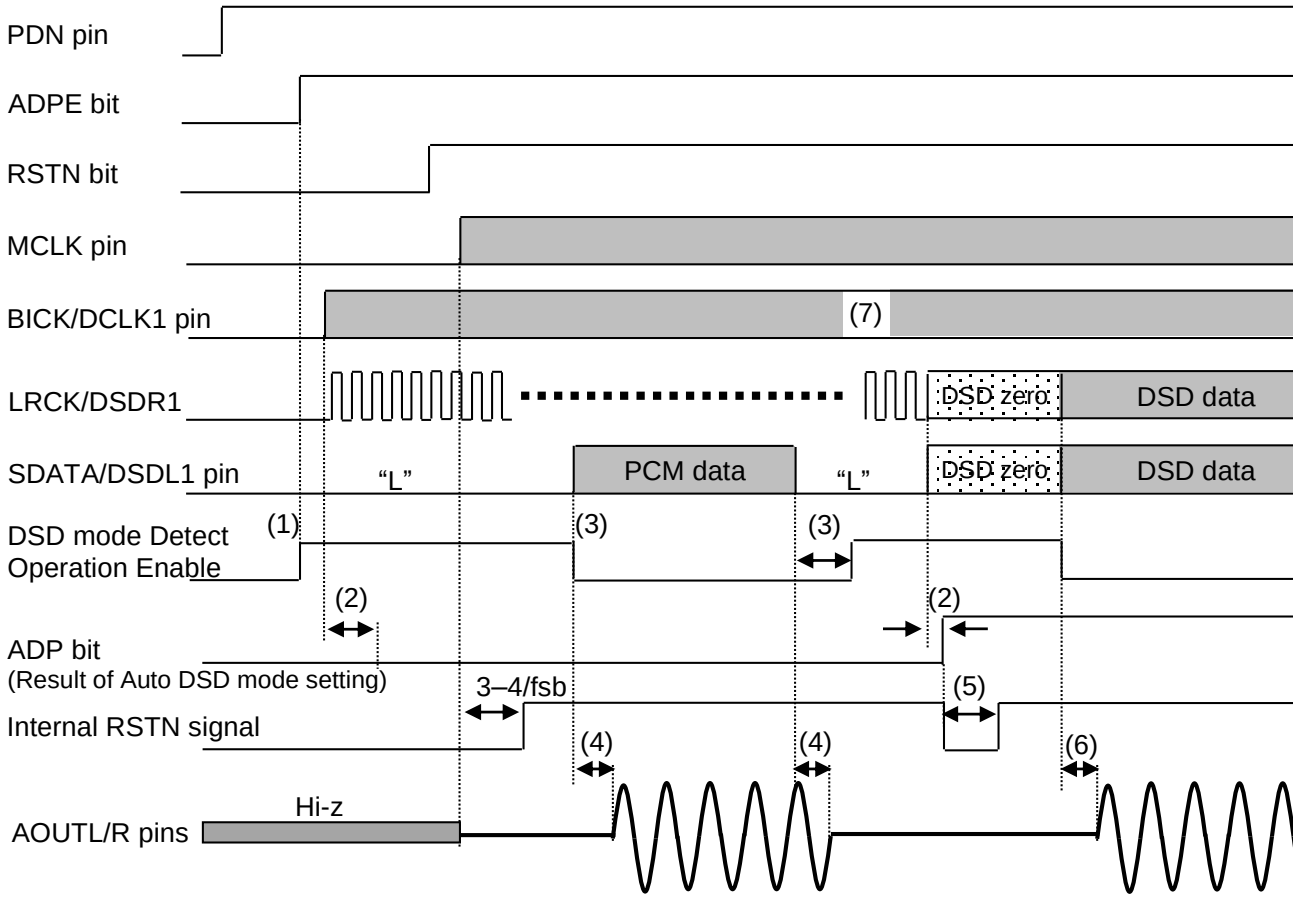
The AK4497S detects mode from the input signal to the LRCK/DSDR1 pin. Input one of “01101001 01101001”, “01010101 01010101”, or “00110011 00110011” zero code patterns continuously to the LRCK/DSDR1 pin when changing to DSD mode from PCM mode (Table 45).

Input a clock that toggles in N times 16 BICK cycles or a clock that is continuously “L” or “H” for 32 BICK cycles or more to the LRCK/DSDR1 pin (Table 45). Refer to Figure 58 and Figure 59 for the operation sequence.
The AK4497S keeps the previous mode instead of executing mode switching if any condition is not satisfied.

Table 45. Input Signal when Switching PCM/DSD mode

LRCK/DSDR1 Pin Input Signal	Detection Result
One of zero code patterns below is input twice consecutively. “01101001 01101001” or “01010101 01010101” or “00110011 00110011”	DSD mode
Clock toggles in N times 16 BICK cycles (N ≥ 1) or Clock that keeps “L” or “H” for 32 BICK cycles	PCM mode

The AK4497S executes data mode detection even if there is no MCLK input while the STBYN bit = “0” or RSTN bit = “0”. However, the analog output becomes Hi-Z and the AK4497S enters standby state when MCLK is stopped. The AK4497S resumes operation according to a data mode that is detected when MCLK is input again. The data mode will be maintained if the input clock to the BICK/DCLK1 pin is stopped.
The AK4497S executes an internal reset for 3–4/fsb automatically when switching the data mode and resumes operation.



Notes:

(1) Automatic mode switching between PCM and DSD modes is enabled by setting the ADPE bit = "1" after setting the PDN pin "L" → "H". If the RSTN bit is in default value "0", mode detection operation will start.

(2) Mode detection is performed by monitoring the input signal code pattern of the LRCK/DSDR1 pin. It is executed for 34 cycles of the BICK/DCLK1 pin input clock and then the ADP bit is changed on a rising edge of the input signal of the LRCK/DSDR1 pin. Mode detection is executed even when there is no MCLK input. The AK4497S starts data mode detection when input data of both channels are zero for a period set by the ADPT[1:0] bits.

(3) The AK4497S finishes data mode detection when any non-zero data is input.

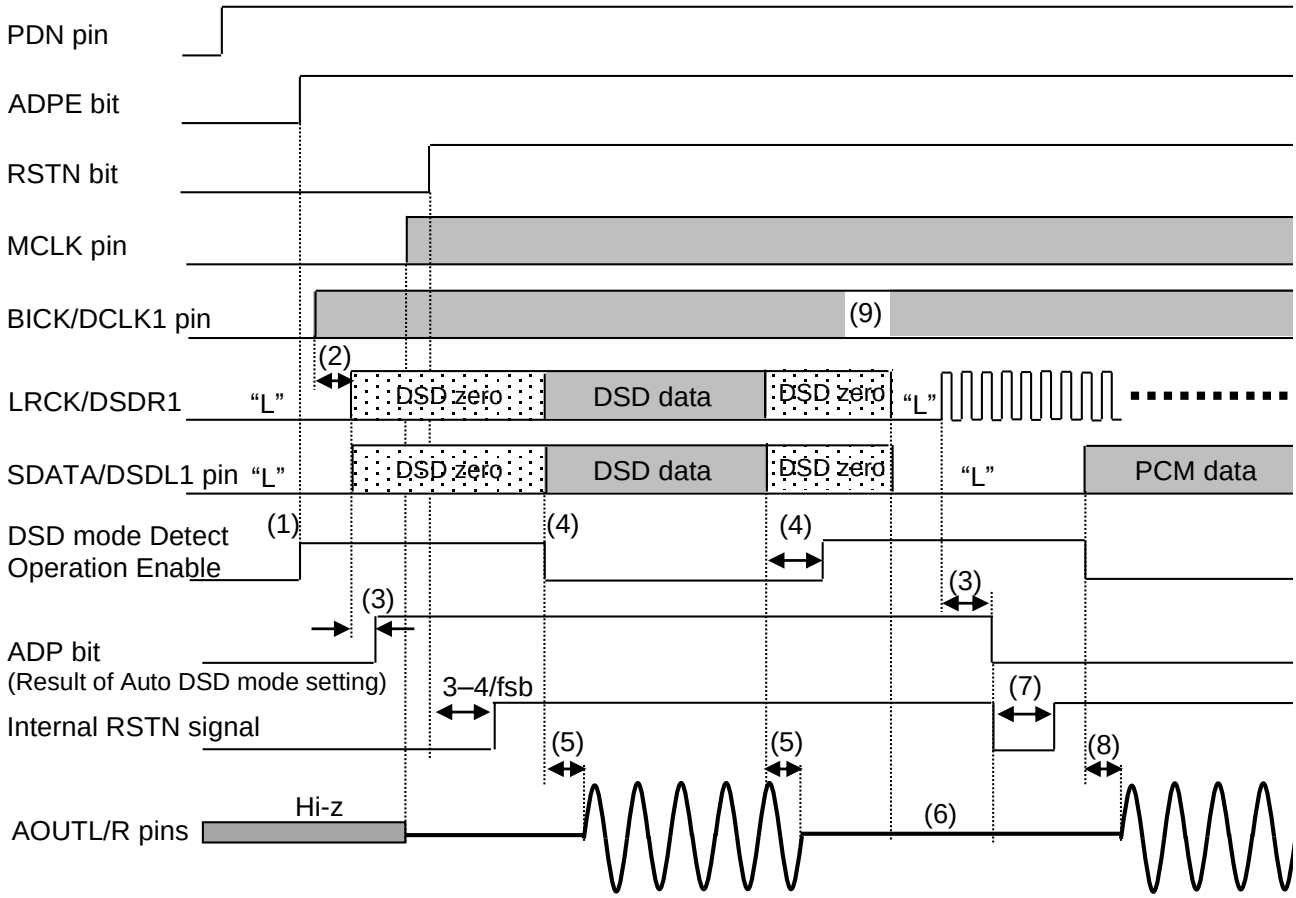
(4) In PCM mode, the analog output delay time becomes 18/fsb longer compared to when setting the ADPE bit = "0".

(5) When the data mode is changed, the AK4497S executes an internal reset for 3–4/fsb automatically.

(6) In DSD mode, the analog output delay time becomes longer compared to when setting the ADPE bit = "0". In this case, the delay time depends on the DDMT bit setting.

(7) A clock input to the BICK/DCLK1 pin is necessary for data mode detection. The data mode will be maintained if the input clock to the BICK/DCLK1 pin is stopped.

Figure 58. Changing to DSD mode after Power up in PCM mode (DSDPATH bit = "1", EXDF bit = "0")



Notes:

(1) Automatic mode switching between PCM and DSD modes is enabled by setting the ADPE bit = "1" after setting the PDN pin "L" → "H". If the RSTN bit is in its default value "0", mode detection operation will start.

(2) Upon power up the AK4497S operates in PCM mode if BICK/DCLK1 is input and SDATA/DSDL1 = "L".

(3) Mode detection is performed by the monitoring input signal code pattern of the LRCK/DSDR1 pin. It is executed for 34 cycles of the BICK/DCLK1 pin input clock and then the ADP bit is changed on a rising edge of the input signal of the LRCK/DSDR1 pin. The ADP bit outputs "0" in PCM mode and "1" in DSD mode. Mode detection is executed even when there is no MCLK input.

(4) The AK4497S finishes data mode detection when any non-zero data is input. Then the AK4497S restarts the mode detection when input data of all channels are continuously zero for the period set by the ADPT[1:0] bits.

(5) In DSD mode, the analog output delay time becomes longer compared to when setting the ADPE bit = "0". In this case, the delay time depends on the DDMT bit setting.

(6) If DSD data input is stopped in DSD mode, the AK4497S stays in DSD mode and continues operation. In this case, full-scale data is input to the AK4497S. Excessive signal output can be avoided by setting the DDM bit = "1" enabling the automatic mute function to operate when detecting a DSD full-scale input.

(7) When the data mode is changed, the AK4497S executes an internal reset for 3–4/fsb automatically.

(8) In PCM mode, the analog output delay time becomes 18/fsb longer compared to when setting the ADPE bit = "0".

(9) A clock input to the BICK/DCLK1 pin is necessary for data mode detection. The data mode will be maintained if the input clock to the BICK/DCLK1 pin is stopped.

Figure 59. Changing to PCM mode after Power up in DSD mode (DSDPATH bit = "1", EXDF bit = "0")

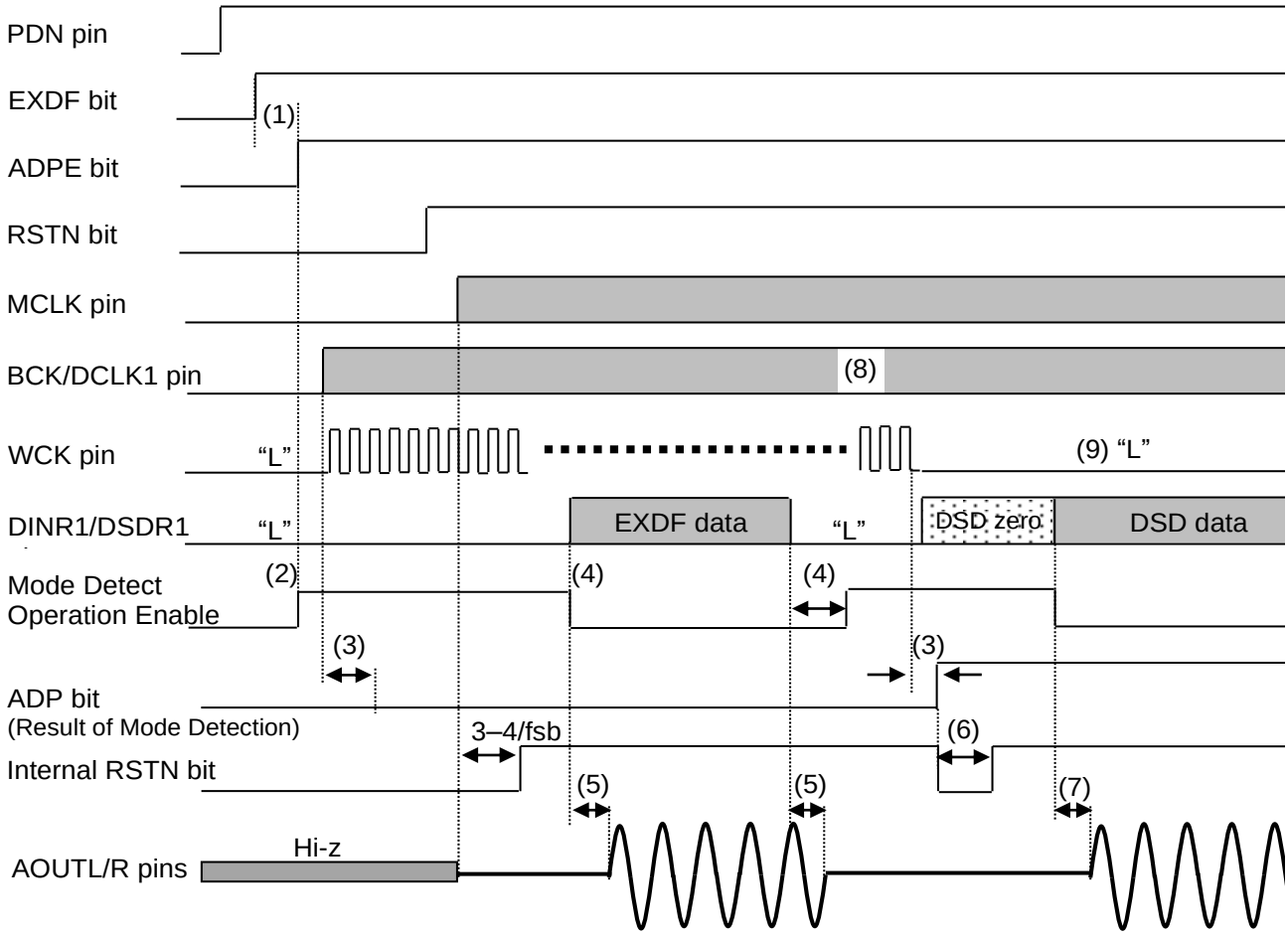
・ EXDF/DSD Automatic Mode Switching (EXDF bit = “1”)

The AK4497S detects the mode from the input clocks to the WCK pin and the BCK/DCLK1 pin. DSD mode is detected if the number of rising edges of the BCK/DCLK1 input clock exceeds 256 times in one cycle of WCK input clock counting from a rising edge. EXDF mode is detected if the number of rising edges of the BCK/DCLK1 input clock does not reach 256 times in one cycle WCK input clock twice consecutively (Table 46). Refer to Figure 60 and Figure 61 for the operation sequence.
The AK4497S keeps its previous mode instead of executing mode switching if any condition is not satisfied.

Table 46. Mode Detection Conditions when Switching EXDF/DSD mode

BCK/DCLK1 Pulse in One WCK Cycle	Detection Result
Once “256 < BCK/DCLK1 pulse number”	DSD mode
Twice Continuously “BCK/DCLK1 pulse number ≤ 256”	EXDF mode

The AK4497S executes data mode detection even if there is no MCLK input while the STBYN bit = “0” or RSTN bit = “0”. However, the analog output becomes Hi-Z and the AK4497S enters standby state when MCLK is stopped. The AK4497S resumes operation according to any data mode that is detected when MCLK is input again. The data mode will be maintained if the input clock to the BCK/DCLK1 pin is stopped.
The AK4497S executes internal reset for 3–4/fsb automatically when switching the data mode and resumes operation.



Notes:

(1) The EXDF bit must be set before setting the ADPE bit.

(2) Automatic mode switching between EXDF and DSD modes is enabled by setting the ADPE bit = "1" after setting the PDN pin "L" → "H". If the RSTN bit is in default value "0", mode detection operation will start.

(3) Mode detection is performed by monitoring the input clock of the WCK pin and the BCK/DCLK1 pin. It takes 256 DCLK1 cycles for mode switching from EXDF to DSD mode and takes 2 WCK cycles for mode switching from DSD to EXDF mode. Mode detection is executed even when there is no MCLK input.

(4) The AK4497S finishes data mode detection when any data that is not zero is input. The AK4497S restarts data mode detection when the input data of both channels are zero for a period set by the ADPT[1:0] bits.

(5) In EXDF mode, the analog output delay time becomes 18/fsb longer compared to when setting the ADPE bit = "0".

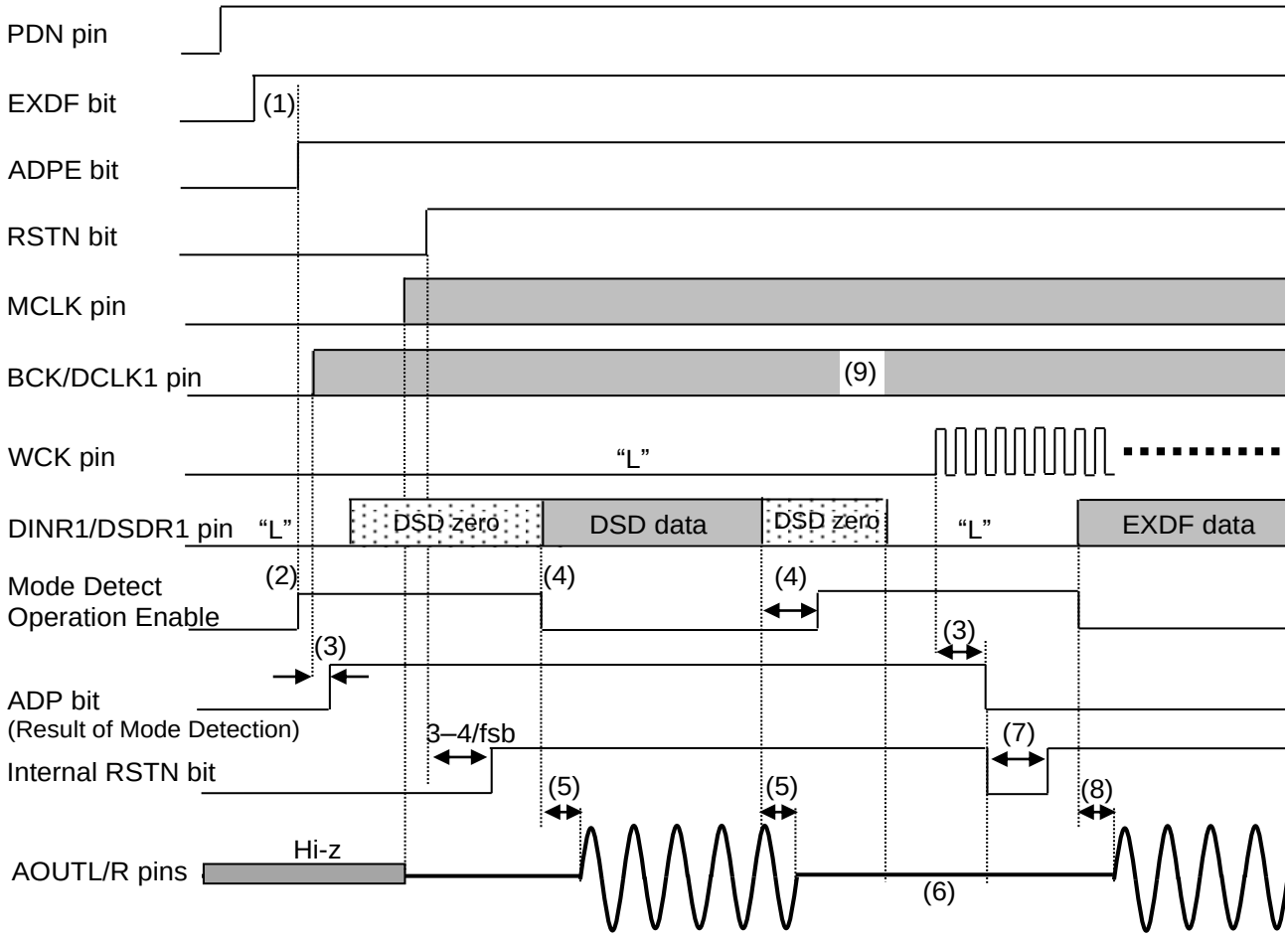
(6) When DSD mode is changed, the AK4497S executes an internal reset for 3–4/fsb automatically.

(7) In DSD mode, the analog output delay time becomes longer compared to when setting the ADPE bit = "0". In this case, the delay time depends on the DDMT bit setting.

(8) A clock input to the BICK/DCLK1 pin is necessary for data mode detection. The data mode will be maintained if the input clock to the BICK/DCLK1 pin is stopped.

(9) WCK input should be "L" when using DSD mode since DSD mode detection is performed by monitoring presence or absence of the WCK input clock when EXDF bit = "1".

Figure 60. Changing to DSD mode after Power up in EXDF mode (DSDPATH bit = "1", EXDF bit = "1")



Notes:

(1) The EXDF bit must be set before setting the ADPE bit.

(2) Automatic mode switching between EXDF and DSD modes is enabled by setting the ADPE bit = "1" after setting the PDN pin "L" → "H". If the RSTN bit is in default value "0", mode detection operation will start.

(3) Mode detection is performed by monitoring the input clock of the WCK pin and the BCK/DCLK1 pin. It takes 256 DCLK1 cycles for mode switching from EXDF to DSD mode, and it takes 2 WCK cycles for mode switching from DSD to EXDF mode. Mode detection is executed even when there is no MCLK input.

(4) The AK4497S finishes data mode detection when any data that is not zero is input. The AK4497S restarts data mode detection when input data of both channels are zero for a period set by the ADPT[1:0] bits.

(5) In DSD mode, the analog output delay time becomes longer compared to when setting the ADPE bit = "0". In this case, the delay time depends on the DDMT bit setting.

(6) If DSDR input is stopped in DSD mode, the AK4497S stays in DSD mode and continues operation. In this case, full-scale data is input to the AK4497S. Excessive signal output can be avoided by setting the DDM bit = "1" enabling the automatic mute function to operate when detecting DSD full-scale input.

(7) When the data mode is changed, the AK4497S executes an internal reset for 3–4/fsb automatically.

(8) In EXDF mode, the analog output delay time becomes 18/fsb longer compared to when setting the ADPE bit = "0".

(9) A clock input to the BICK/DCLK1 pin is necessary for data mode detection. The data mode will be maintained if the input clock to the BICK/DCLK1 pin is stopped.

Figure 61. Changing to EXDF mode after Power up in DSD mode (DSDPATH bit = "1", EXDF bit = "1")

9.16. Soft Mute Operation (PCM mode, DSD mode, EXDF mode)

Soft mute operation is performed at digital domain. When the SMUTE pin is set to “H” or the SMUTE bit is set to “1”, the attenuation level softly transitions from the current level to MUTE (−∞ dB). After that, when the SMUTE pin is set to “L” or the SMUTE bit is set to “0”, the attenuation level returns from MUTE to the level set by the ATTL/R[7:0] bits by soft transition. The transition speed is determined by the ATS bit setting. If the soft mute is cancelled before attenuating to −∞ dB, the soft mute is discontinued and returned to attenuation level set by the ATTL/R[7:0] bits in the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.
The soft mute function is not available when bypassing the volume (DSDD bit = “1”) in DSD mode.

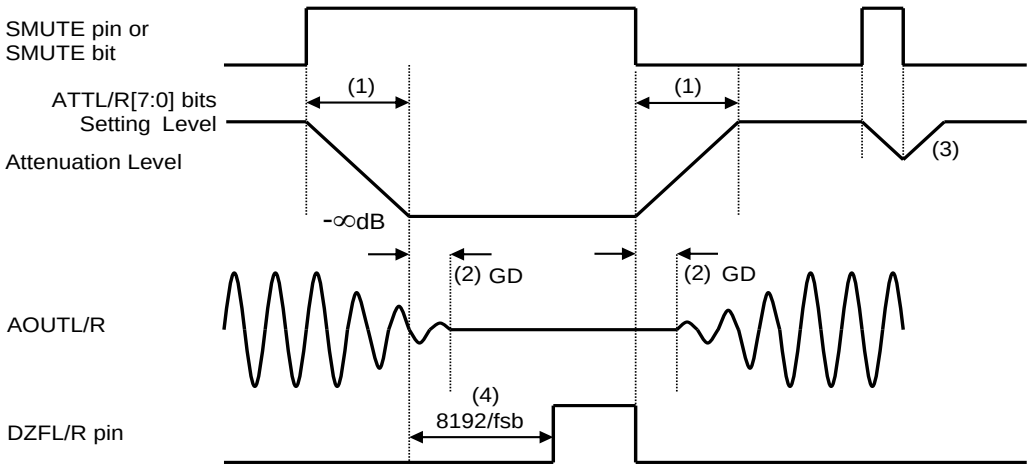


Figure 62. Soft Mute Function

Notes:

(1) (255 − ATTL/R[7:0] bits setting) × Transition time per 0.5 dB.
Transition time per 0.5 dB = (Transition Time in Table 31) / 255
For example, this time is 4080/fsb at ATTL/R[7:0] bits = 255 in PCM mode.

(2) The analog output corresponding to the digital input has group delay (GD).

(3) If the soft mute is cancelled before attenuating to -∞ dB, the soft mute is discontinued and returned to attenuation level set by the ATTL/R[7:0] bits in the same cycle.

(4) When the input data for each channel is continuously zeros for 8192/fsb (16384/fsb in DSD512 mode), the DZFL/R pin for each channel goes to “H”. The DZFL/R pins immediately return to “L” if input data are not zero.

9.17. LDO

When TVDD = 3.0 to 3.6 V, the power for digital core circuit (DVDD) is supplied by the internal LDO by setting the LDOE pin to “H”. Table 47 shows the DVDD pin statuses with the PDN and LDOE pins setting. The internal LDO is powered up by setting the PDN pin from “L” to “H” (power down release) and it starts supplying 1.8 V (typ.) DVDD. It takes 0.1 ms (max.) to power up the internal LDO.

Table 47. LDO Select Mode

PDN pin	LDOE pin	TVDD Voltage	Internal LDO	DVDD pin State
*	L	1.7 – 3.6 V	OFF	Power Supply Input Pin Supply 1.7 to 1.98 V externally.
L	H	3.0 – 3.6 V	OFF	Internally pulled down by 500Ω.
H	H	3.0 – 3.6 V	ON	Capacitor Connection Pin (Output 1.8 V (typ.)) Do not connect DVDD with other devices.

(*: Do not care)

The AK4497S has an error detect function as shown in Table 48 for LDO operation (LDOE pin = “H”). The internal LDO will be powered down and stop supplying the power to the digital core when an error is detected. In this case, the analog signal output and the SDA pin (In I^2C-bus mode) becomes Hi-Z state (ACK is not output). The AK4497S must be reset by setting the PDN pin = “L” → “H” to recover from the error detection state.

Table 48. Error Detection

No.	Error Detection	Error Detection Conditions
1	LDO Overvoltage Detection	The AK4497S detects an error when the output voltage of the LDO pin exceeds overvoltage threshold. Threshold: 2.35 V (typ.)
2	LDO Overcurrent Detection	The AK4497S detects an error when the current flows from LDO output exceeds overcurrent threshold. Threshold: 54 mA (typ.)

9.18. Analog Output Heavy Load Drive

When the HLOAD Pin = “H” in Pin Control mode, or the HLOAD bit = “1” in Register Control mode, analog output pins AOUTLP/LN and AOUTRP/RN can drive 120 Ω (min.) load resistance (vs. ground), thus suppressing S/N ratio degradation due to thermal noise from external circuits. See Note 17, Figure 83 and Figure 84.

9.19. Analog Output Overcurrent Protection

Analog output pins AOUTLP/LN and AOUTRP/RN have channel independent overcurrent protection. When any current that exceeds 120 mA (typ.) is output from any of these analog output pins, this function limits the output not to exceed 120 mA (typ.). This function is invalid when the PDN pin = “L”, STBYN bit = “0”, MSTBN bit = “0” or MCLK is stopped.

When the current becomes overcurrent and the current is limited, the analog signal continues to be output, but the output waveform is clipped. If the current value returns to below 120 mA (typ.) after this Over Current Protection function has been activate, the device will return to normal operation.

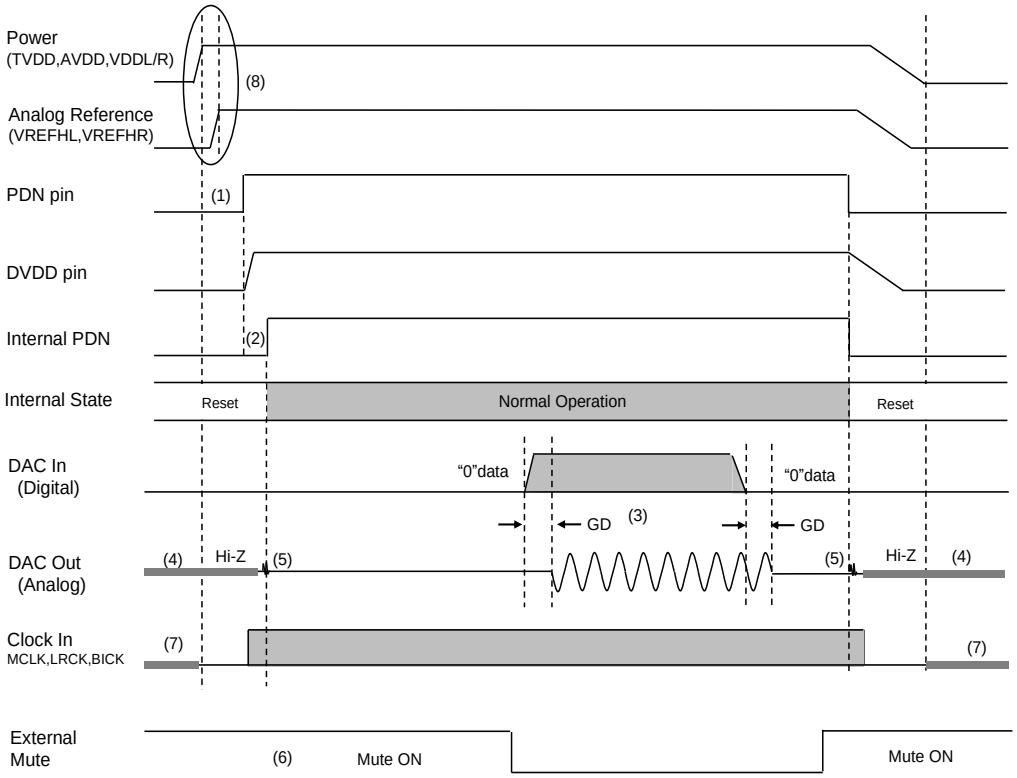
9.20. Power Up/Down Function

The AK4497S is powered down when the PDN pin is “L”. In power down state, all circuits stop operation and are initialized, and the analog output becomes floating (Hi-Z) state. The PDN pin must held “L” for more than 150 ns for a certain reset after all power supplies are on. There is a possibility of malfunctions with the “L” pulse less than 150 ns. Power down is released by setting the PDN pin to “H” from “L”. The analog output becomes floating (Hi-Z) state until all clocks are input.

When not using the internal LDO (LDOE pin = “L”), TVDD must be powered up before DVDD or at the same time. Other than that, there are no restrictions on the order of power-up. The internal LDO outputs DVDD (1.8 V (typ.)) when the LDOE pin = “H”. Also, there are no restrictions on the order of power-up.

9.20.1. Pin Control mode (PSN pin = “H”)

All circuits will be powered up by inputting MCLK, LRCK and BICK clocks after the PDN pin = “H”. Figure 63 shows system timing example of power up/down when using the internal LDO (LDOE pin “H”).

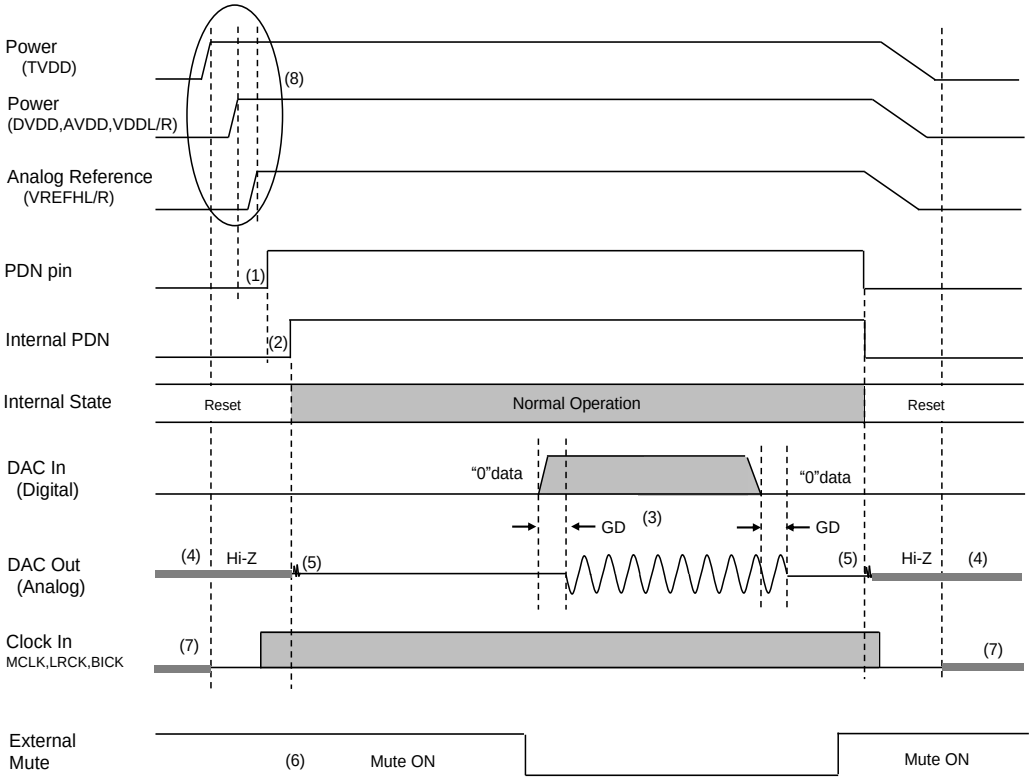


Notes:

(1) The PDN pin must be “L” when start supplying AVDD, TVDD and VDDL/R. It must be held “L” for more than 150 ns after AVDD, TVDD and VDDL/R are powered up.
(2) The internal LDO is powered up after the PDN pin = “H” if the LDOE pin = “H”. The internal circuit will start operation (max. 2 ms later) after the PDN pin = “H”.
(3) The analog output corresponding to the digital input has group delay (GD).
(4) Analog outputs are floating (Hi-Z) in power down mode.
(5) Click noise occurs on an edge of the PDN signal. This noise is output even if “0” data is input.
(6) Mute the analog output externally if click noise (5) adversely affects system performance.
(7) Do not input clocks (MCLK, BICK and LRCK) until after the power supplies are turned on.
(8) VREFHL/R must be powered up after or at the same time as VDDL/R.

Figure 63. Power up/down Sequence Example (Pin Control mode, LDOE pin = “H”)

The timing example when not using the internal LDO (LDOE pin = “L”) is shown in Figure 64.
When the LDOE pin = “L”, TVDD must be powered up before or at the same time as the DVDD.



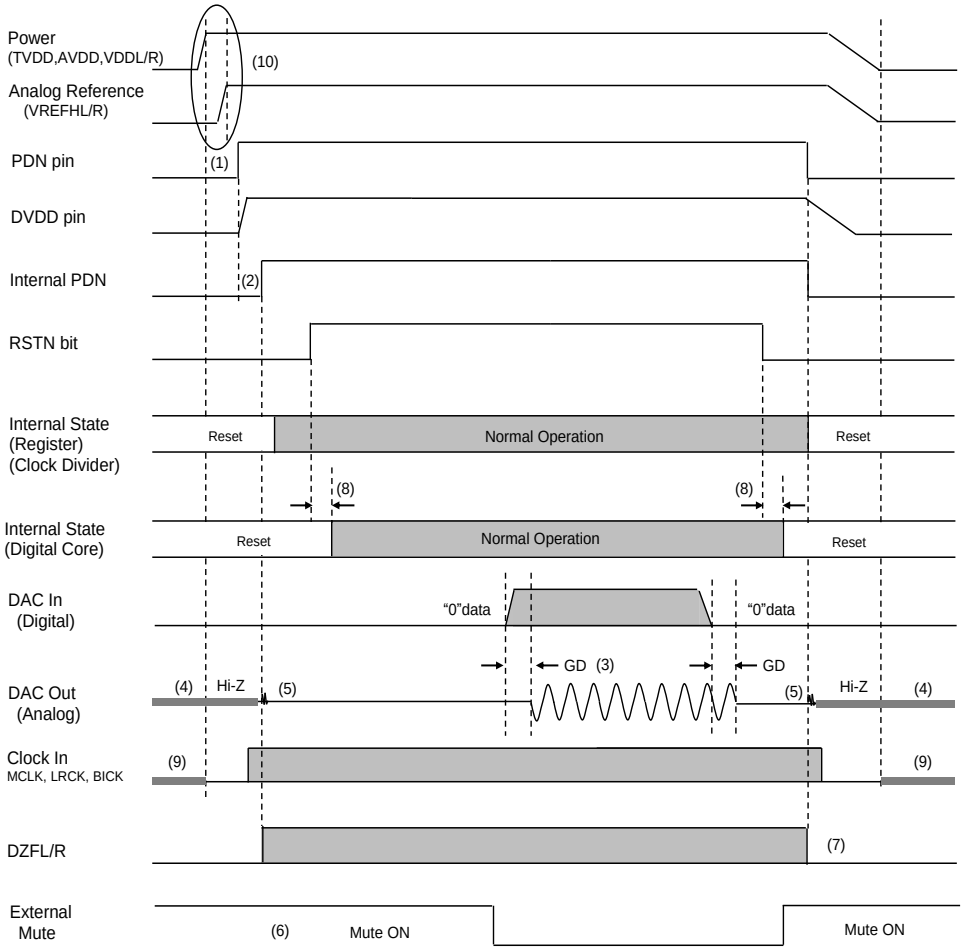
Notes:

(1) The PDN pin must be “L” when start supplying AVDD, TVDD, DVDD and VDDL/R. It must be held “L” for more than 150 ns after AVDD, TVDD, DVDD and VDDL/R are powered up.
(2) In case the LDOE pin = “L”, the internal circuit will start operation (max. 1 μs later) after the PDN pin = “H”.
(3) The analog output corresponding to the digital input has group delay (GD).
(4) The analog outputs are floating (Hi-Z) in power down mode.
(5) Click noise occurs on an edge of the PDN signal. This noise is output even if “0” data is input.
(6) Mute the analog output externally if click noise (5) adversely affects system performance.
(7) Do not input clocks (MCLK, BICK and LRCK) until the power supplies are turned on.
(8) TVDD must be powered up before or at the same time as DVDD. VREFHL/R must be powered up after or at the same time as VDDL/R.
(9) TVDD must be powered down after or at the same time as the DVDD. Power down sequences of other power supplies are not critical.

Figure 64. Power up/down Sequence Example (Pin Control mode, LDOE pin = “L”)

9.20.2. Register Control mode (PSN pin = “L”)

Figure 65 shows system timing example of power up/down when using the internal LDO (LDOE pin = “H”). Register access becomes available and internal LDO is powered up after setting the PDN pin = “H”. The analog circuit starts operation by supplying necessary clocks (MCLK, LRCK and BICK for PCM mode, MCLK and DCLK for DSD mode, MCLK, BCK and WCK for EXDF mode) and the clock divider is powered up about after 4/fsb. In this time, the analog output pins output analog common voltages (VCML, VCMR). Then the AK4497S transitions to normal operation by setting the RSTN bit = “1”.

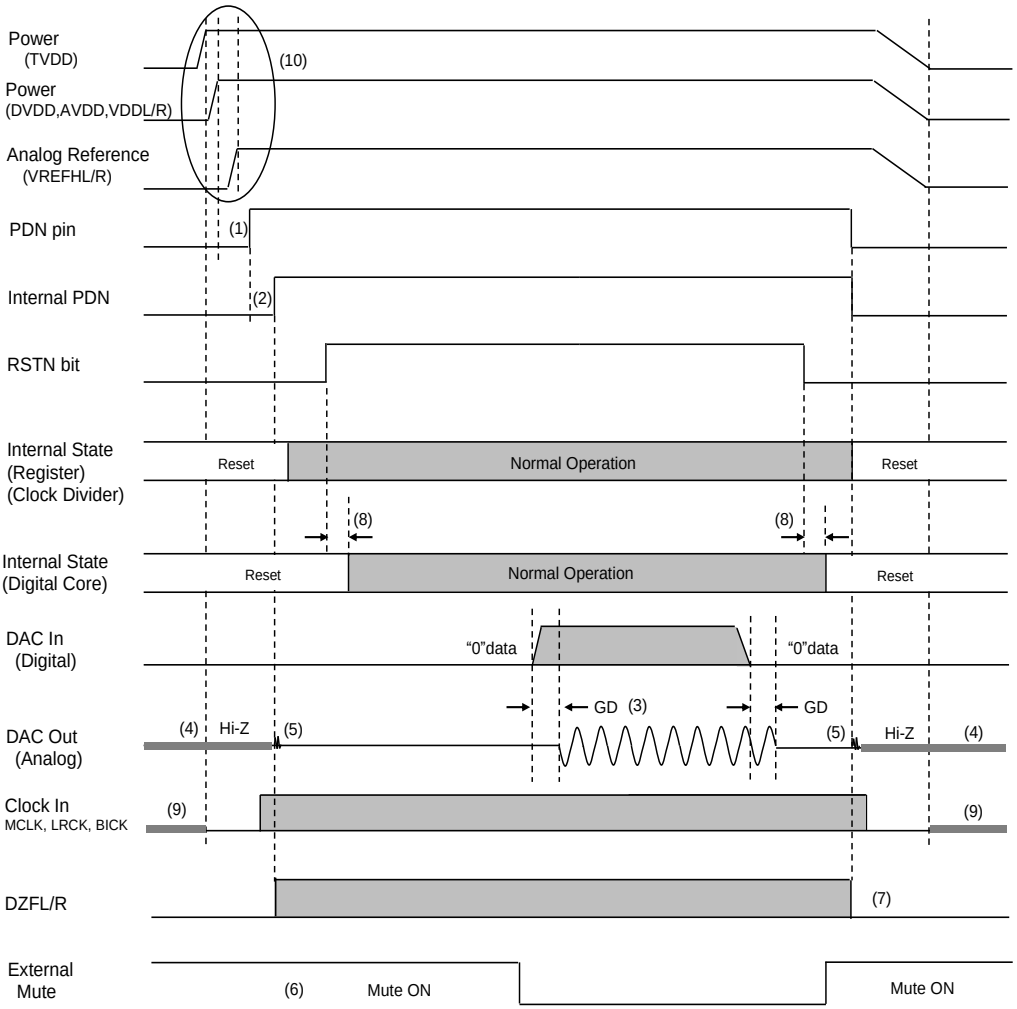


Notes:

(1) The PDN pin must be “L” when start supplying AVDD, TVDD and VDDL/R. It must be held “L” for more than 150 ns after AVDD, TVDD and VDDL/R are powered up.
(2) The internal LDO is powered up after the PDN pin = “H” if the LDOE pin = “H”. The internal circuit will start operation (max. 2 ms later) after the PDN pin = “H”.
(3) The analog output corresponding to the digital input has group delay (GD).
(4) The analog outputs are floating (Hi-Z) in power down mode.
(5) Click noise occurs on an edge of the PDN signal. This noise is output even if “0” data is input.
(6) Mute the analog output externally if click noise (5) adversely affects system performance.
(7) The DZFL/R pin is “L” in power down mode (PDN pin = “L”).
(8) It takes 3/fsb to 4/fsb until a reset instruction is valid when writing the RSTN bit to “0” and it takes 3/fsb to 4/fsb when releasing the reset.
(9) Do not input clocks (MCLK, BICK and LRCK) until the power supplies are turned on.
(10) VREFHL/R must be powered up after or at the same time as VDDL/R.

Figure 65. Power up/down Sequence Example (Register Control Mode, LDOE pin = “H”)

The system timing example of power up/down when not using the LDO (LDOE pin = “L”) is shown in Figure 66. When the LDOE pin = “L”, TVDD must be powered up before or at the same time as DVDD.



Notes:

(1) The PDN pin must be “L” when start supplying AVDD, TVDD, DVDD and VDDL/R. It must be held “L” for more than 150 ns after AVDD, TVDD, DVDD and VDDL/R are powered up.
(2) In case the LDOE pin = “L”, the internal circuit will start operation (max. 1 μs later) after the PDN pin = “H”.
(3) The analog output corresponding to the digital input has group delay (GD).
(4) The analog outputs are floating (Hi-Z) in power down mode.
(5) Click noise occurs at the edge of PDN signal. This noise is output even if “0” data is input.
(6) Mute the analog output externally if click noise (5) adversely affects system performance.
(7) The DZFL/R pin is “L” in power down mode (PDN pin = “L”).
(8) It takes 3/fsb to 4/fsb until the internal RSTN state is changed when changing the RSTN bit to “0” and it takes 3/fsb to 4/fsb when changing the RSTN bit to “1”.
(9) Do not input clocks (MCLK, BICK and LRCK) until the power supplies are turned on.
(10) TVDD must be powered up before or at the same time as DVDD. VREFHL/R must be powered up after or at the same time as VDDL/R. Power up sequence of other power supplies are not critical.
(11) TVDD must be powered down after or at the same time as DVDD. Power down sequences of other power supplies are not critical.

Figure 66. Power up/down sequence example (Register Control mode, LDOE pin = “L”)

9.21. Power Down/Standby/Reset Function

Power Down, Standby and Reset function of the AK4497S are controlled by the STBYN bit, RSTN bit and MCLK (Table 49).

Table 49. Power Down, Standby, Reset Function

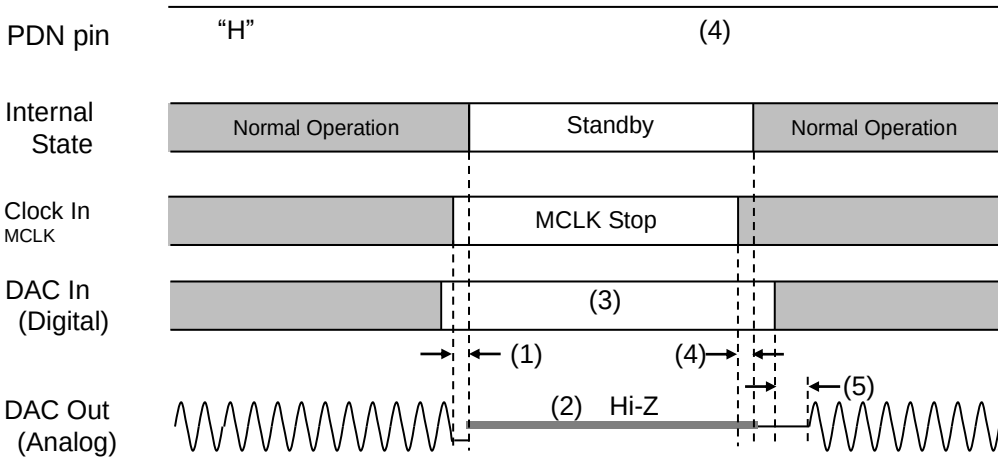
Mode	PDN Pin	MCLK Supply	STBYN bit	RSTN bit	Digital Block	Analog Block	LDO and Registers	Analog Output
Power Down	L	*	*	*	OFF	OFF	OFF	Hi-Z
Standby (MCLK Stop) (Note 51)	H	No	*	*	OFF	OFF	ON	Hi-Z
Standby (STBYN bit = "0")	H	Yes	0	*	OFF	OFF	ON	Hi-Z
Reset	H	Yes	1	0	OFF	ON	ON	VCML/R
Normal Operation	H	Yes	1	1	ON	ON	ON	Signal output

(*: Do not care)

Note 51. This standby mode is valid in case the MSTBN bit = "0". This standby mode is set by the condition of the PDN pin and STBYN bit in case the MSTBN bit = "1".

9.21.1. Standby by stopping MCLK

The AK4497S has an MCLK stoppage detection circuit. If MCLK is not input for 1 μs (min.) during normal operation (PDN pin = "H"), the device is into standby mode. In standby mode, all circuits except the MCLK stoppage detection circuit, control registers, bias generation circuit and LDO (only when the LDOE pin = "H") stop operation. In this standby mode, the analog output goes floating (Hi-Z) state. The AK4497S returns to normal operation if the STBYN bit and RSTN bit are "1" after starting to supply MCLK again. The zero detect function is disabled when MCLK is stopped.



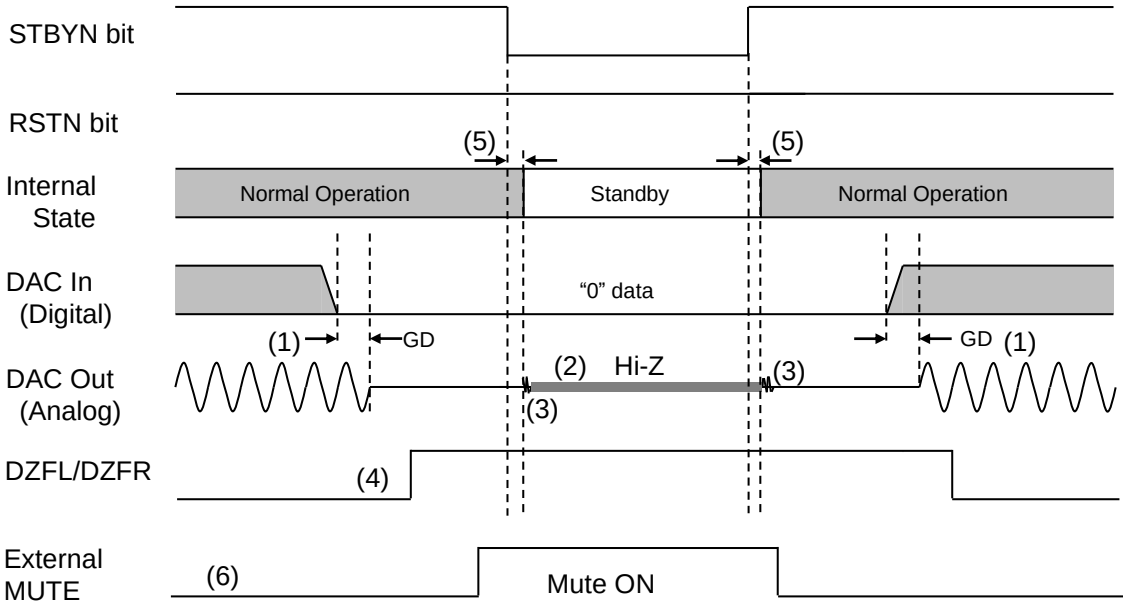
Notes:

(1) The AK4497S detects MCLK stoppage and becomes in standby mode when an MCLK edge is not detected for more than 1 μs during operation.
(2) The analog output goes to floating (Hi-Z) state.
(3) Click noise can be reduced by inputting "0" data when stopping and resuming MCLK supply.
(4) Resume MCLK input to release the standby mode by MCLK. In this case, power up sequence by the PDN pin or standby sequence by the STBYN bit is not necessary.
(5) The analog output corresponding to the digital input has group delay (GD).

Figure 67. Standby Sequence Example by MCLK

9.21.2. Standby by STBYN bit

All circuits except for the control registers, bias generation circuit and LDO (only when the LDOE pin = “H”) stop operation by setting the STBYN bit to “0”. At this time, control register access is available. The analog output goes to floating (Hi-Z) state. Figure 68 shows the standby sequence by the STBYN bit.



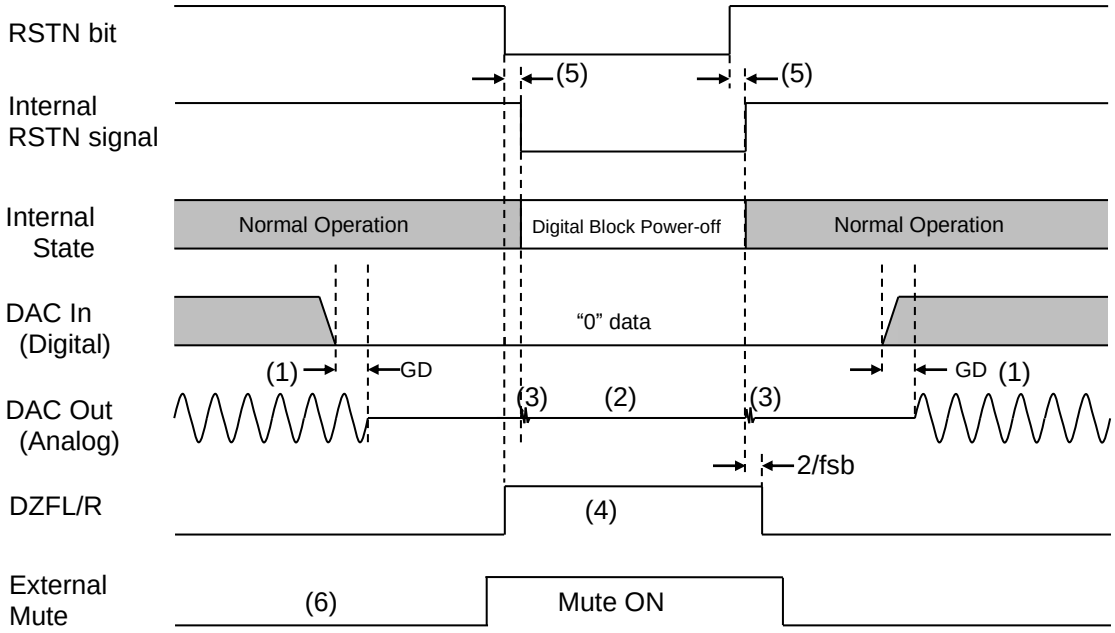
Notes:

(1) Input “0” data before entering standby mode. The analog output corresponding to the digital input has group delay (GD).
(2) The AK4497S becomes in standby mode when the STBYN bit is set to “0”. The analog output is floating (Hi-Z) in standby mode.
(3) Click noise occurs when the internal state switched. This noise is output even if “0” data is input.
(4) The zero detection function is also valid during standby. This figure shows the sequence when the DZFE bit = “1”, DZFB bit = “0” and DZFM bit = “0”.
(5) It takes 2/fsb to 3/fsb when switching the internal state.
(6) Mute the analog output externally if click noise or Hi-Z output adversely affect system performance.

Figure 68. Standby Sequence Example by STBYN bit

9.21.3. Reset by the RSTN bit

Digital circuits except for the control registers and clock divider are reset by setting the RSTN bit to “0”. In this case, the control register settings are held, the analog output becomes VCML/R voltage and the DZFL/R pin outputs “H”. Figure 69 shows the reset sequence by the RSTN bit.



Notes:

(1) Input “0” data before entering reset mode. The analog output corresponding to the digital input has group delay (GD).
(2) The AK4497S becomes in reset mode when the RSTN bit = “0”. The analog output is VCML/R voltage in reset mode.
(3) Click noise occurs on the edge of the internal RSTN signal. This noise is output even if “0” data is input.
(4) The DZFL/R pin goes “H” on the falling edge of the RSTN signal and goes “L” 2/fsb after the rising edge of the internal RSTN signal. This figure shows the sequence when the DZFE bit = “1”, DZFB bit = “0” and DZFM bit = “0”.
(5) It takes 3/fsb to 4/fsb until the internal RSTN is changed when changing the RSTN bit to “0” and it takes 3/fsb to 4/fsb when changing the RSTN bit to “1”.
(6) Mute the analog output externally if click noise adversely affects system performance.

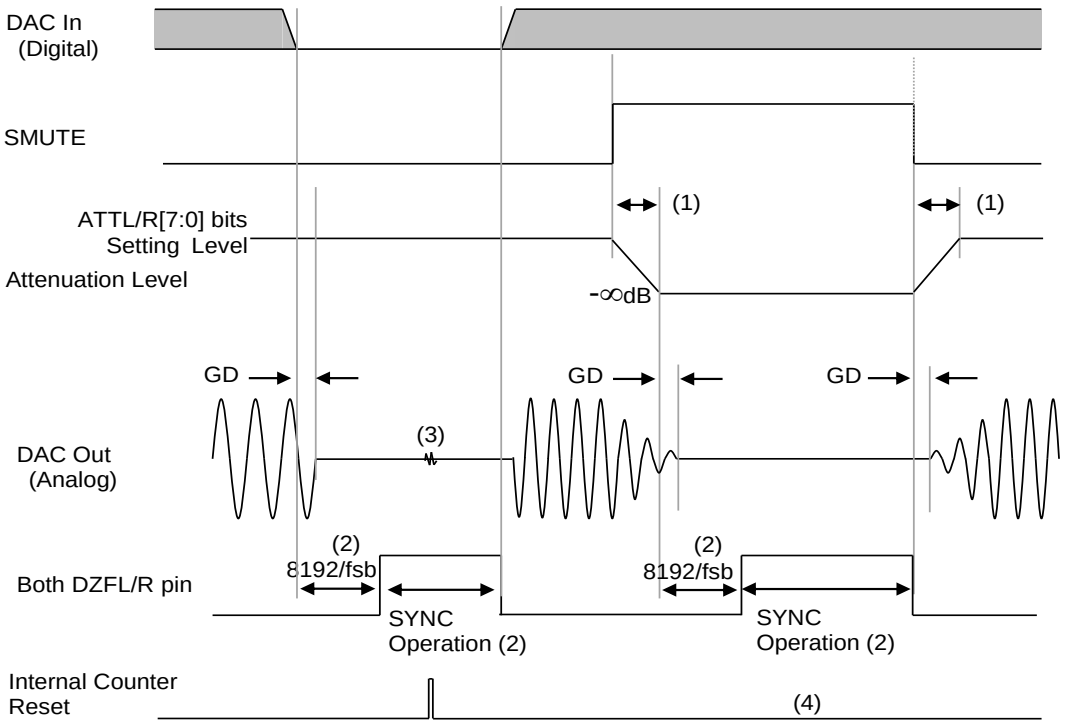
Figure 69. Reset Sequence Example by RSTN bit

9.22. Synchronize Function (PCM, EXDF)

The AK4497S has a function that resets the internal counter to keep the timing of the falling edge of the internal clock and the external clock edge within a certain range. With this synchronize function, group delays between each device can be kept within 4/256fsb when using multiple pieces of AK4497S.

The clock synchronize function becomes valid when input data of both L and R channels are “0” for 8192 times continuously in PCM mode or EXDF mode, when both L and R channels become “0” and kept for 8192 times continuously by attenuation or when the RSTN bit = “0”. In PCM mode, the internal counter is synchronized with a rising edge of LRCK (falling edge of LRCK in I²S mode), and it is synchronized with a rising edge of WCK in EXDF mode. In this case, the analog output has the same voltage as VCML/R.

This function is disabled by setting the SYNCE bit = “0” in register control mode. Figure 70 shows a synchronizing sequence when the input data is “0” for 8192 times continuously. Figure 71 shows a synchronizing sequence by the RSTN bit.



Note:

(1) Regarding ATT Transition time, refer to Table 31.

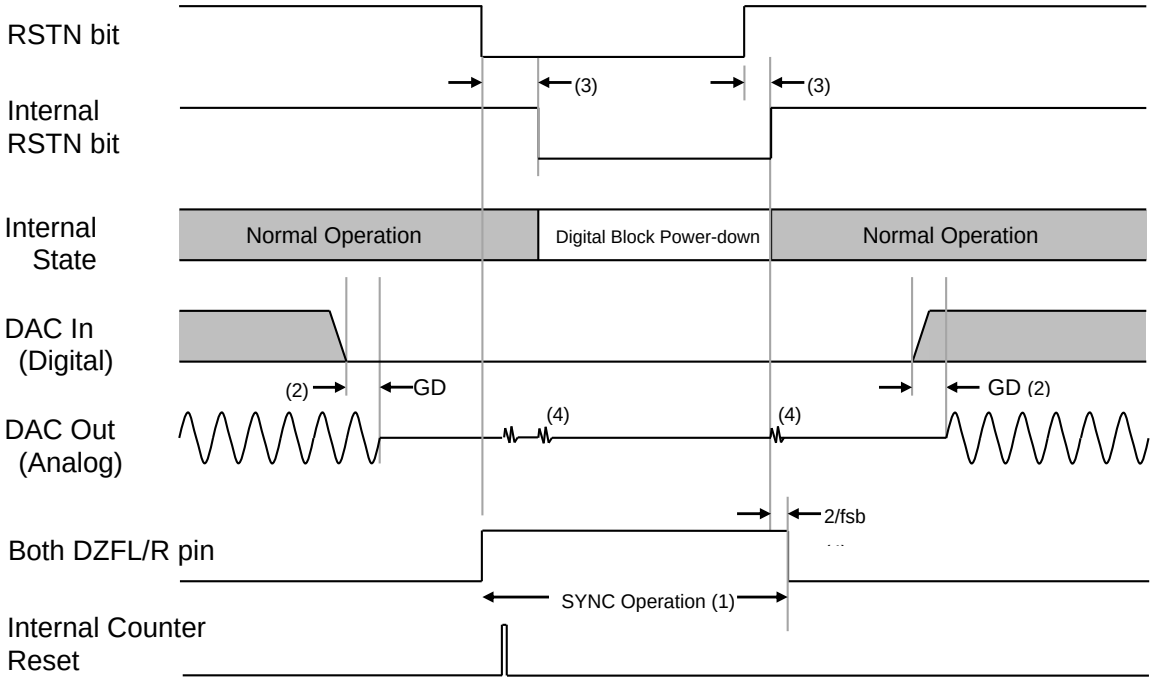
(2) When both the L and R channels data are “0” for 8192 times continuously, the DZFL and DZFR pins become “H” and the synchronize function is valid.

(3) Click noise may occur when the internal counter is reset. This noise is output even if “0” data is input. Mute the analog output externally if this click noise affects the system performance.

(4) When the internal clock and external clock are in synchronization, the internal counter is not reset even if the synchronize function is valid.

Figure 70. Synchronizing Sequence by Continuous “0” Data Input for 8192 Times

If the RSTN bit is set to “0”, the output signal of the DZFL/R pin becomes “H”. Then, the DAC is reset after 3/fsb to 4/fsb and the analog output becomes the same voltage as VCML/R. The synchronize function becomes valid when both the DZFL and DZFR pins output “H”.



Note:

(1) The DZFL and the DZFR pins become “H” by a falling edge of the RSTN bit, and becomes “L” in 2/fsb after a rising edge of the internal signal of the RSTN bit. The synchronize function is valid during the DZFL/R pin = “H”.

(2) Since the analog output corresponding to digital input has group delay (GD), it is recommended to have a no-input period longer than the group delay before writing “0” to the RSTN bit.

(3) It takes 3/fsb to 4/fsb until the internal RSTN is changed when changing the RSTN bit to “0” and it takes 3/fsb to 4/fsb when changing the RSTN bit to “1”. The synchronization function becomes valid immediately when writing “0” to the RSTN bit. Therefore, there is a case that the internal counter is reset before the internal RSTN signal of the device is changed.

(4) Click noise occurs on the rising and falling edges of the internal RSTN signal and when the internal counter is reset. This noise is output even if “0” data is input. Mute the analog output externally if this click noise affects the system performance.

(5) To ensure synchronization, keep the reset state for at least 500 μs after the synchronization function is enabled.

Figure 71. Synchronization Sequence by RSTN Bit

9.23. Control Register Interface

In Register Control mode, the register interface can be selected from 3-wire serial or I²C-bus by the I2C pin.

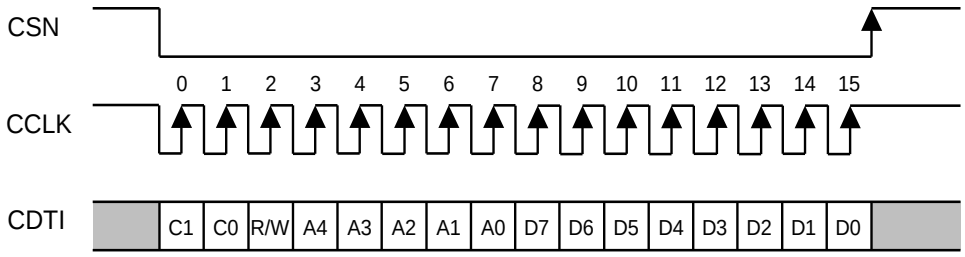
Table 50. Control Register Interface Mode Select

I2C pin	Register Interface Mode
L	3-wire Serial mode
H	I²C-bus mode

Setting the PDN pin to “L” resets the registers to their default values. In register control mode, the digital block except control registers and clock divider is reset by setting the RSTN bit to “0”. In this case, the register values are not initialized.

9.23.1. 3-wire Serial Control mode (I2C pin = “L”)

The control registers are written to via the CSN, CCLK and CDTI pins. The data on this interface consists of Chip address (2-bit, C1/0), Read/Write (1-bit; fixed to “1”, write only), Register address (MSB first, 5-bit) and Control data (MSB first, 8-bit). The data is received on a rising edge of CCLK. The received data is written into the register by rising edge of CSN. The maximum frequency of CCLK is 5 MHz.



C1-C0: Chip Address (C1 bit =CAD1 pin, C0 bit =CAD0 pin)
R/W: READ/WRITE (Fixed to “1”, Write only)
A4-A0: Register Address
D7-D0: Control Data

Figure 72. Control I/F Timing

Notes:
(1) The AK4497S does not support read commands in 3-wire serial control mode.
(2) When the AK4497S is in power down mode (PDN pin = “L”), writing into control registers is prohibited.
(3) The received data cannot be written when the number of CCLK rising edges is 15 times or less, or 17 times or more during the framing interval where CSN is “L”.

9.23.2. I²C-bus Control mode (I2C pin = “H”)

The AK4497S supports the fast-mode I²C-bus.

9.23.2.1. WRITE Operation

Figure 73 shows the data transfer sequence for the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 79). After the START condition, a slave address is sent. This address is 7-bit long followed by the eighth bit that is a data direction bit (R/W). The most significant five bits of the slave address are fixed as “00100”. The next bits are CAD1 and CAD0 (device address bits). This bit identifies the specific device on the bus. The hard-wired input pin (CAD1 pin, CAD0 pin) sets these device address bits (Figure 74). If the slave address matches that of the AK4497S, the AK4497S generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 80). A R/W bit value of “1” indicates that the read operation is to be executed, and “0” indicates that the write operation is to be executed.

The second byte consists of sub address corresponding to the control register address of the AK4497S and the format is MSB first. The most significant three bits must be fixed as “000” (Figure 75). The data after the second byte contains control data. The format is MSB first, 8-bit (Figure 76). The AK4497S generates an acknowledge after receiving each byte. Data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 79).

The AK4497S can perform more than one byte write operation per sequence. After receipt of the third byte the AK4497S generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet, the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds “15H” prior to generating a stop condition, the address counter will “roll over” to “00H” and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW (Figure 81) except for the START and STOP conditions.

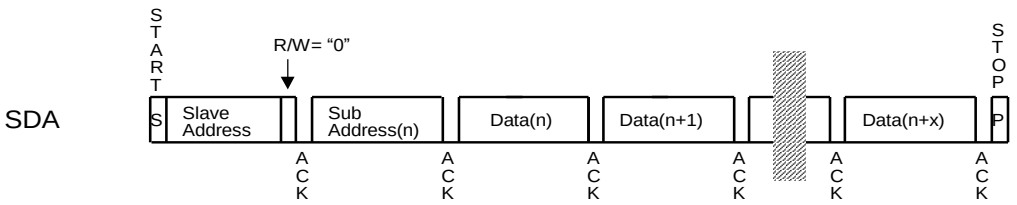


Figure 73. Data Transfer Sequence in I²C-bus mode

0	0	1	0	0	CAD1	CAD0	R/W

(CAD0 and CAD1 are set by pins)

Figure 74. The First Byte

0	0	0	A4	A3	A2	A1	A0

Figure 75. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 76. Byte Structure after The Second Byte

9.23.2.2. READ Operation

Set the R/W bit = “1” for the READ operation of the AK4497S. After transmission of data, the master can read the next address’s data by generating an acknowledge instead of terminating the read cycle after the receipt of the first data word. After sending each data packet, the internal address counter is incremented by one, and the next data is automatically sent to the master. If the address exceeds “15H” prior to receiving stop condition, the address counter will “roll over” to “00H” and the data of “00H” will be read out.

The AK4497S supports two basic read operations: Current Address Read and Random Address Read.

Current Address Read

The AK4497S has an internal address counter that maintains the address of the last accessed register incremented by one. Therefore, if the last access (either a read or write) were to address “n”, the next current address read operation would access data from the address “n+1”. After receipt of the slave address with R/W bit “1”, the AK4497S generates an acknowledge, transmits 1-byte data of the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge (NACK) and generates a stop condition, the AK4497S ceases the transmission.

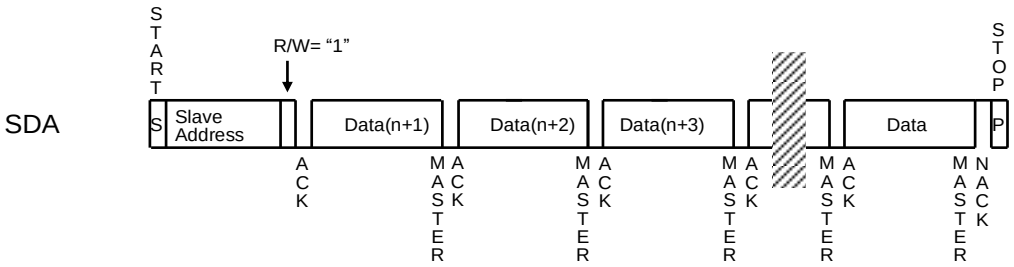


Figure 77. Current Address Read

Random Address Read

The random read operation allows the master to access any address at random. Prior to issuing the slave address with the R/W bit “1”, the master must first perform a “dummy” write operation. The master issues a start condition, a slave address (R/W bit = “0”) and then the register address to read. After the register address is acknowledged, the master immediately reissues the start condition and the slave address with the R/W bit “1”. The AK4497S then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge (NACK) and generates a stop condition, the AK4497S ceases the transmission.

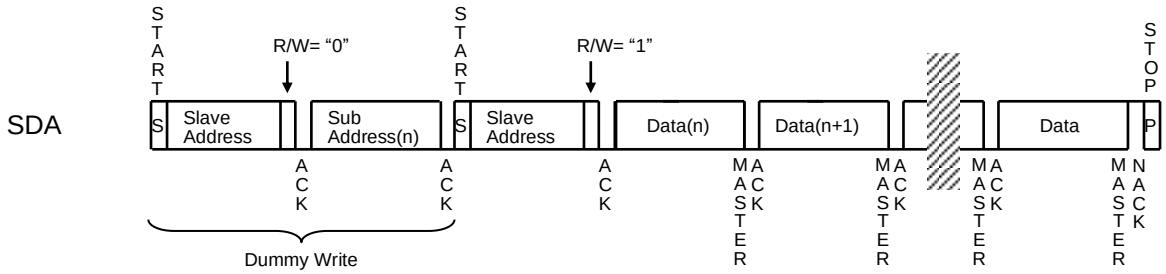


Figure 78. Random Address Read

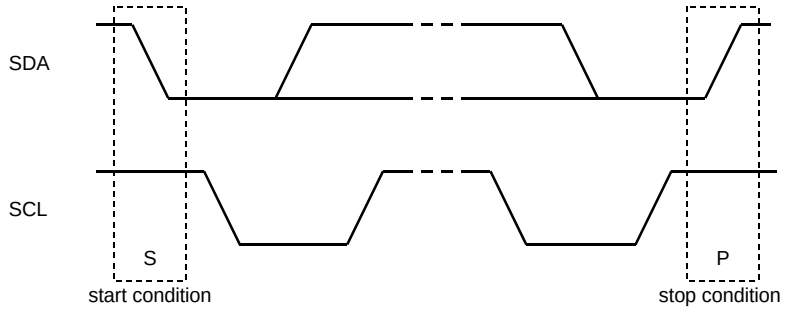


Figure 79. Start Condition and Stop Condition

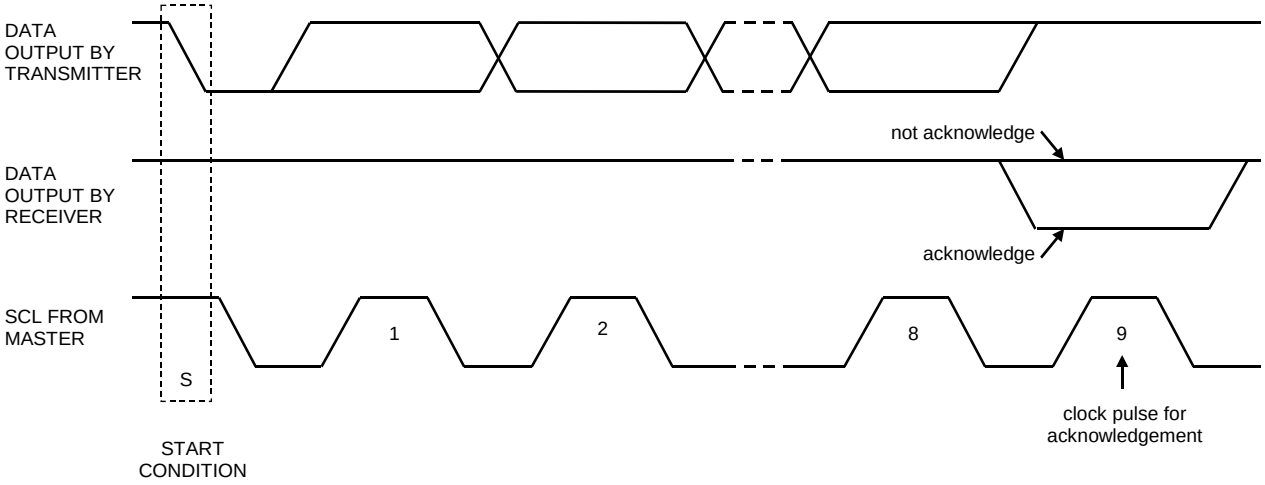


Figure 80. Acknowledge (I^2C-bus)

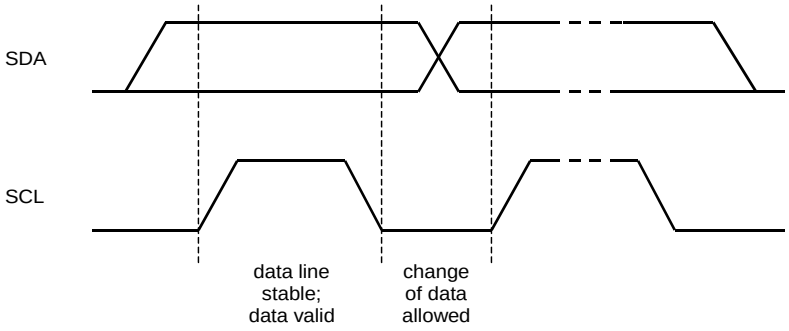


Figure 81. Bit Transfer (I^2C-bus)

9.24. Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	EXDF	ECS	AFSD	DIF2	DIF1	DIF0	RSTN
01H	Control 2	DZFE	DZFM	SD	DFS1	DFS0	DEM1	DEM0	SMUTE
02H	Control 3	DP	ADP	DCKS	DCKB	MONO	DZFB	SELLR	SLOW
03H	L-ch ATT	ATTL7	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
04H	R-ch ATT	ATTR7	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0
05H	Control 4	INVL	INVR	0	0	0	0	DFS2	SSLOW
06H	DSD1	DDM	DML	DMR	DDMOE	DDMT1	DDMT0	DSDD	DSDSEL0
07H	Control 5	MSTBN	0	0	0	GC2	GC1	GC0	SYNCE
08H	Sound Control	0	0	0	0	HLOAD	SC2	SC1	SC0
09H	DSD2	0	0	0	0	0	DSDPATH	DSDF	DSDSEL1
0AH	Control 6	TDM1	TDM0	SDS1	SDS2	0	STBYN	0	0
0BH	Control 7	ATS1	ATS0	0	SDS0	0	0	DCHAIN	TEST
0CH	Reserved	0	0	0	0	0	0	0	0
0DH	FIR CRAM Setting	0	0	0	0	0	CRAMR	CRAMW	CRAM CLR
0EH	FIR tap address	FIRT7	FIRT6	FIRT5	FIRT4	FIRT3	FIRT2	FIRT1	FIRT0
0FH	FIRC[23:16]	FIRC23	FIRC22	FIRC21	FIRC20	FIRC19	FIRC18	FIRC17	FIRC16
10H	FIRC[15:8]	FIRC15	FIRC14	FIRC13	FIRC12	FIRC11	FIRC10	FIRC09	FIRC08
11H	FIRC[7:0]	FIRC07	FIRC06	FIRC05	FIRC04	FIRC03	FIRC02	FIRC01	FIRC00
12H	RFIRC[23:16]	RFIRC23	RFIRC22	RFIRC21	RFIRC20	RFIRC19	RFIRC18	RFIRC17	RFIRC16
13H	RFIRC[15:8]	RFIRC15	RFIRC14	RFIRC13	RFIRC12	RFIRC11	RFIRC10	RFIRC09	RFIRC08
14H	RFIRC[7:0]	RFIRC07	RFIRC06	RFIRC05	RFIRC04	RFIRC03	RFIRC02	RFIRC01	RFIRC00
15H	ADFS Read	ADPE	ADPT1	ADPT0	0	0	ADFS2	ADFS1	ADFS0

Notes:

(1) In 3-wire serial control mode, the AK4497S does not support read commands.
(2) The AK4497S supports read command in I^2C-bus control mode.
(3) If the address exceeds “15H” by automatic increment function in I^2C-bus mode, the address counter will “roll over” to “00H” and the next write/read address will be “00H”.
(4) TEST bit on the address 0BH (D0) and bits indicated as 0 in each address must be set to “0”. Malfunctions may occur if writing “1” value to these bits.
(5) Writing after 16H is forbidden. Malfunctions may also occur by this action.
(6) When the PDN pin goes to “L”, the registers are initialized to their default values.
(7) When RSTN bit is set to “0”, the digital blocks except control registers and clock divider are reset, and the registers are not initialized to their default values.
(8) When the PSN pin state is changed, the AK4497S should be reset by the PDN pin.

9.25. Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	EXDF	ECS	AFSD	DIF2	DIF1	DIF0	RSTN
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	1	0	0

RSTN: Internal Timing Reset
0: Reset (default) All registers are not initialized.
1: Normal Operation

DIF[2:0]: Audio Serial Data Interface Modes (Table 22)
Initial value is “110” (Mode 6: 32-bit MSB justified)

AFSD: Sampling Frequency Auto Detect mode Enable (PCM & EXDF mode only) (Table 5)
0: Disable Manual or Auto Setting mode (default)
1: Enable fs Auto Detect mode
(When AFSD bit = “1”, DFS[2:0] bits are ignored.)

ECS: EXDF mode Clock Frequency Setting (Table 21)
0: WCK = 768 kHz (default)
1: WCK = 384 kHz

EXDF: External Digital Filter mode Enable
0: Disable PCM mode (default)
1: Enable External Digital Filter mode

ACKS: Master Clock Frequency Auto Setting mode Enable (PCM & EXDF mode only).(Table 5)
0: Disable Manual Setting mode (default)
1: Enable Auto Setting mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Control 2	DZFE	DZFM	SD	DFS1	DFS0	DEM1	DEM0	SMUTE
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	0	0	0	1	0

SMUTE: Soft Mute Enable
0: Normal Operation (default)
1: DAC outputs soft-muted.

DEM[1:0]: De-emphasis Filter Control (Table 28)
Default = “01” (OFF).

DFS[1:0]: Sampling Speed Mode Select (Lower 2-bits of DFS[2:0]) (Table 10)
Default = “000” (Normal Speed)
(Click noise occurs when DFS[2:0] bits are changed.)

SD: Short Delay Filter Enable. (Table 26)
0: Traditional filter (SSLOW = 0)
Super Slow Roll-off (SSLOW = 1)
1: Short delay filter (SSLOW = 0; default)
Low Dispersion filter (SSLOW = 1)

DZFM: Data Zero Detect Mode
0: Individual L/R channel mode (default)
1: Channel ANDed mode

DZFE: Data Zero Detect Enable
0: Disable (default)
1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Control 3	DP	ADP	DCKS	DCKB	MONO	DZFB	SELLR	SLOW
R/W		R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SLOW: Slow Roll-off Filter Enable (Table 26)
0: Sharp Roll-off filter (default)
1: Slow Roll-off filter

SELLR: The Data Channel Select (Table 36)
MONO bit = "0"
0: Normal (default)
1: Swap L channel and R channel
MONO bit = "1"
0: Both analog channels output L channel data. (default)
1: Both analog channels output R channel data.

DZFB: Polarity Inversion of Zero Detection Flag (Table 35)
0: DZFL/R pin goes "H" at Zero Detection (default)
1: DZFL/R pin goes "L" at Zero Detection

MONO: MONO mode Enable
0: Stereo mode (default)
1: MONO mode

DCKB: Polarity Inversion of DCLK (DSD mode only)
0: DSD data begins on DCLK falling edge. (default)
1: DSD data begins on DCLK rising edge.

DCKS: MCLK Frequency Select (DSD mode only)
0: 512fsb (default)
1: 768fsb

ADP: Read Back Register for Internal D/A Conversion Mode
0: PCM mode or EXDF mode
1: DSD mode

DP: D/A Conversion Mode Select
0: PCM mode or EXDF mode (default)
1: DSD mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	L-ch ATT	ATTL7	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
04H	R-ch ATT	ATTR7	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	1	1	1	1

ATTL[7:0]: Attenuation Level of L channel setting (Table 30)
ATTR[7:0]: Attenuation Level of R channel setting (Table 30)
Default = FFH (0 dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Control 4	INVL	INVR	0	0	0	0	DFS2	SSLOW
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SSLOW: Super Slow Roll Off or Low Dispersion Filter Enable. (Table 26)
0: Disable (default)
1: Enable (see also SD)

DFS2: Sampling Speed Mode Select (Upper 1-bit of DFS[2:0]) (Table 10)
Default = “000” (Normal Speed)

INVR: AOUTR Output Phase Inverting
0: Normal (default)
1: Invert

INVL: AOUTL Output Phase Inverting
0: Normal (default)
1: Invert

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	DSD1	DDM	DML	DMR	DDMOE	DDMT1	DDMT0	DSDD	DSDSEL0
R/W		R/W	R	R	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DSDSEL0: DSD Sampling Speed Select (Lower 1-bit of DSDSEL[1:0]) (Table 20)
Default = “00” (DSD64)

DSDD: DSD Playback Path Select
0: Normal Path (default)
1: Volume Bypass

DDMT[1:0]: DSD Signal Full-scale Detection Time Select (Table 40)
Default = “00” (256 DCLK Cycles)

DDMOE: DSD Full-scale Detection Flag Output to DZFL/R pins Enable (Table 41)
0: Disable (default)
1: Enable

DMR/DML: DSD Full-scale Detection Flag
0: Not Full-Scale (default)
1: Full-Scale

DDM: DSD Data Mute by Full-Scale Detection Enable
0: Disable (default)
1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	Control 5	MSTBN	0	0	0	GC2	GC1	GC0	SYNCE
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	1

SYNCE: Synchronize Function Enable
0: Disable
1: Enable (default)

GC[2:0]: PCM, EXDF, DSD mode Gain Select (Table 33)
Default = "000"

MSTBN: Automatic Standby by stopping MCLK Enable
0: Enable (default)
1: Disable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Sound Control	0	0	0	0	HLOAD	SC2	SC1	SC0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SC[2:0]: Sound Quality Setting (Table 38, Table 39)
Default = "000"

HLOAD: Heavy Load mode Enable
0: Disable (default)
1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	DSD2	0	0	0	0	0	DSDPATH	DSDF	DSDSEL1
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DSDSEL1: DSD Sampling Speed Select (Upper 1-bit of DSDSEL[1:0]) (Table 20).
Default = "00" (DSD64)

DSDF: Cut-off Frequency of DSD Filter Select (Table 27)
0: 39 kHz (@fsb=44.1 kHz, DSD64) (default)
1: 76 kHz (@fsb=44.1 kHz, DSD64)

DSDPATH: DSD Data Input Pin Select
0: DSDL2, DSDR2, DCLK2 pins (default)
1: DSDL1, DSDR1, DCLK1 pins

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	Control 6	TDM1	TDM0	SDS1	SDS2	0	STBYN	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	1	0	0

STBYN: Standby State Control
0: Standby
1: Normal Operation (default)

SDS[2:1]: Data Slot Select (Upper 2-bit of SDS[2:0]) (Table 23)
Default = “000” (L1 and R1 Slot)

TDM[1:0]: Input Mode Select (Table 22)
Default = “00” (Normal mode)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	Control 7	ATS1	ATS0	0	SDS0	0	0	DCHAIN	TEST
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

TEST: Test mode for manufacture
“0” must be written to this bit. Otherwise, malfunctions may occur.

DCHAIN: Daisy Chain mode Enable
0: Disable (default)
1: Enable

SDS[0]: Data Slot Select (Lower 1-bit of SDS[2:0]) for TDM mode (Table 23)
Default = “000” (L1 and R1 Slot)

ATS[1:0]: Attenuation Level Transition Speed Select (Table 31)
Default = “00” (Min. Speed)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	Reserved	0	0	0	0	0	0	0	0
R/W		R	R/W	R/W	R/W	R	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

0CH: Reserved

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0DH	FIR CRAM Setting	0	0	0	0	0	CRAMR	CRAMW	CRAMCLR
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

CRAMCLR: CRAM Data Clear
0: Not Cleared (default)
1: Set Initial Value

CRAMW: CRAM Data Write Enable
0: Disable (default)
1: Enable

CRAMR: CRAM Data Read Enable
0: Disable (default)
1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0EH	FIR Tap Address	FIRT7	FIRT6	FIRT5	FIRT4	FIRT3	FIRT2	FIRT1	FIRT0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

FIRT[7:0]: Tap Address Setting
Default = “00H”

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0FH	FIRC[23:16]	FIRC23	FIRC22	FIRC21	FIRC20	FIRC19	FIRC18	FIRC17	FIRC16
10H	FIRC[15:8]	FIRC15	FIRC14	FIRC13	FIRC12	FIRC11	FIRC10	FIRC09	FIRC08
11H	FIRC[7:0]	FIRC07	FIRC06	FIRC05	FIRC04	FIRC03	FIRC02	FIRC01	FIRC00
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

FIRC[23:0]: FIR Coefficient Setting
Default = “000000H”

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
12H	RFIRC[23:16]	RFIRC 23	RFIRC 22	RFIRC 21	RFIRC 20	RFIRC 19	RFIRC 18	RFIRC 17	RFIRC 16
13H	RFIRC[15:0]	RFIRC 15	RFIRC 14	RFIRC 13	RFIRC 12	RFIRC 11	RFIRC 10	RFIRC 09	RFIRC 08
14H	RFIRC[7:0]	RFIRC 07	RFIRC 06	RFIRC 05	RFIRC 04	RFIRC 03	RFIRC 02	RFIRC 01	RFIRC 00
R/W		R	R	R	R	R	R	R	R
Default		0	0	0	0	0	0	0	0

RFIRC[23:0]: FIR Coefficient Readout
Default = “000000H”

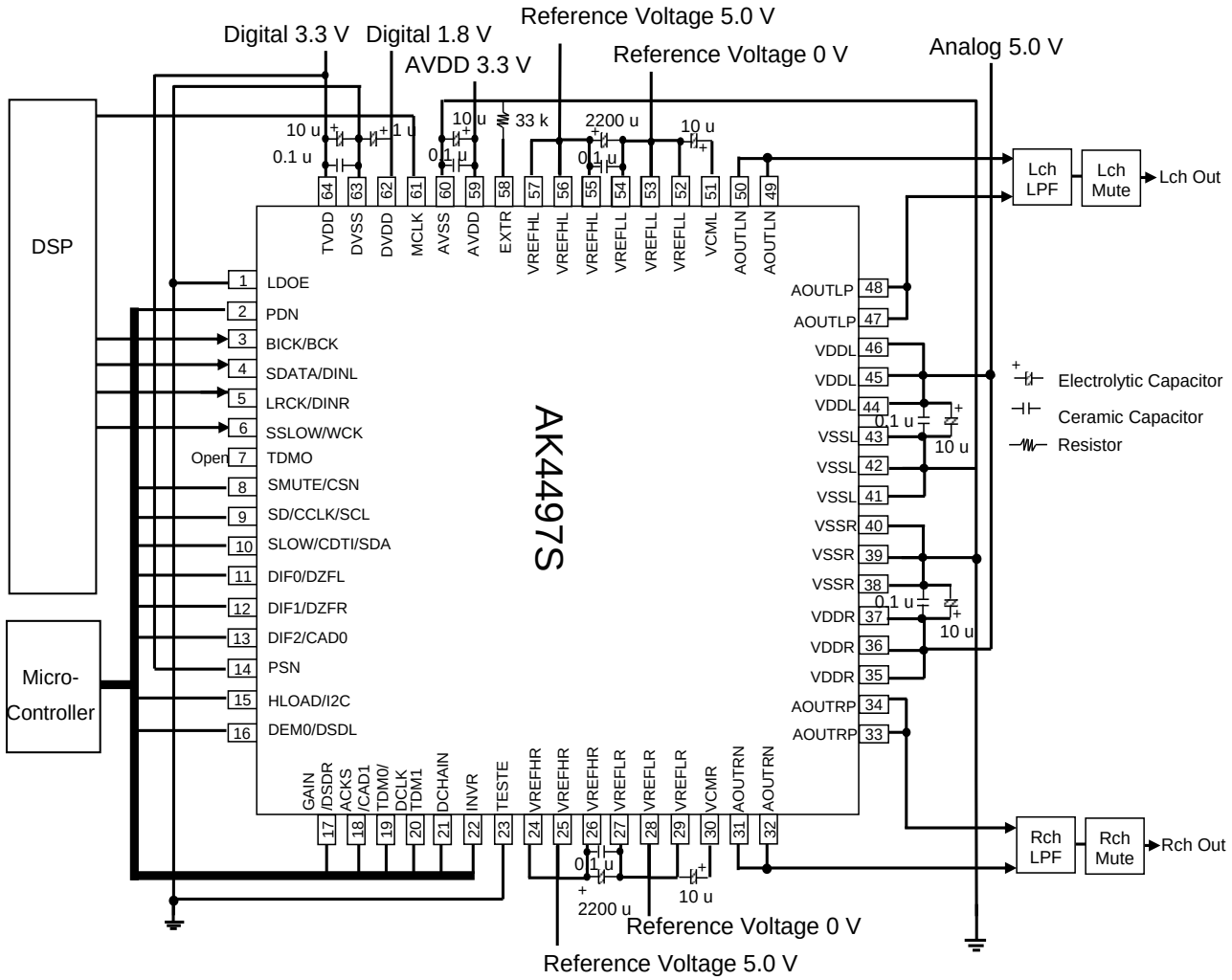
Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
15H	ADFS Read	ADPE	ADPT1	ADPT0	0	0	ADFS2	ADFS1	ADFS0
R/W		R/W	R/W	R/W	R/W	R/W	R	R	R
Default		0	0	0	0	0	0	0	0

ADFS[2:0]: Sampling Speed Mode Detection Result in fs Auto Detect mode (Table 18)
Default = “000” (Normal Speed mode)

ADPT[1:0]: Zero Data Duration Select for Starting Conversion Mode Detection (Table 44).
Default = “00” (Longest)

ADPE: Automatic PCM/DSD Conversion Mode Switching Enable
0: Disable (default)
1: Enable

10. Recommended External Circuits



Notes:

- Power lines of AVDD, DVDD, TVDD, VDDL and VDDR should be distributed separately from the point with low impedance of regulator etc.
- AVSS, DVSS, VSSL and VSSR must be connected to the same analog ground plane. (Analog ground should has low impedance as a solid pattern. THD+N characteristics will degrade if there are impedances between each VSS.)
- It is recommended to connect a damping resistor if THD+N characteristics degrade by high frequency noise of MCLK.
- All input pins except pull-down/pull-up pins should not be allowed to float.

Figure 82. Typical Connection Diagram
(AVDD = TVDD = 3.3 V, DVDD = 1.8 V, VDDL/R = 5.0 V, LDOE pin = “L”, Pin Control mode)

10.1. Grounding and Power Supply Decoupling

To minimize coupling by digital noise, decoupling capacitors should be connected to AVDD, TVDD, DVDD, VDDL and VDDR. AVDD and VDDL/R are supplied from analog supply in system, and TVDD and DVDD are supplied from digital supply in system. Power lines of VDDL/R should be distributed separately from the point with low impedance of regulator etc. When not using LDO (LDOE pin = "L"), power supplies should be powered up in the order of 3.3 V power supplies (AVDD, TVDD) first, the 1.8 V power supply (DVDD) next and 5 V power supplies (VDDL/R) last. When using LDO (LDOE pin = "H"), the internal LDO outputs 1.8 V. **AVSS, DVSS, VSSL and VSSR must be connected to the same analog ground plane.** Decoupling capacitors for high frequency should be placed as near as possible to the supply pin.

10.2. Voltage Reference

The differential voltage between VREFHL/R and VREFLL/R sets the full scale of the analog output range. The VREFHL/R pin is normally connected to the 5.0 V reference voltage, and the VREFLL/R pin is normally connected to the 0 V reference voltage. VREFHL/R and VREFLL/R should be connected with a 0.1 µF ceramic capacitor and a 2200 µF electrolytic capacitor as near as possible to the pin to eliminate the effects of high frequency noise.
The VREFH and VREFL pins should be treated to not have noises from other supply pins. If the analog characteristics cannot satisfy the specification by this noise, connect the VREFH to analog 5.0 V via a 10 Ω resistor and connect the VREFL pin to the analog ground via a 10 Ω resistor. (A low-pass filter of fc = 500 Hz will be composed by a 2200 µF capacitor and a 10 Ω resistor. This low-pass filter removes signal frequency noise from other power supply pins.)
VCML/R is a common voltage of this chip. No load current may be drawn from the VCML/R pin. All signals, especially clocks, should be kept away from the VREFHL/R and VREFLL/R pins in order to avoid unwanted noise coupling into the AK4497S.

10.3. Analog Outputs

The analog outputs are full differential outputs. The differential outputs are summed externally, V_{AOUT} = (AOUT+) − (AOUT-) between AOUTLP/RP and AOUTLN/RN. If the summing gain is 1, the output range of the setting the GAIN pin = "L" or GC[2] bit = "0" is ±2.8 Vpp (typ., VREFHL/R − VREFLL/R = 5 V) centered around VCML and VCMR voltages. In this case, the output range after summing will be 5.6 Vpp (typ.). The output range of the setting the GAIN pin = "H" or GC[2] bit = "1" is ±3.75 Vpp (typ.) centered around VCML and VCMR voltages. In this case, the output range after summing will be 7.5 Vpp (typ.). The bias voltage of the external summing circuit is supplied externally.

The input data format is 2's complement. The output voltage (V_{AOUT}) is a positive full scale for 7FFFFFFFH (@32-bit) and a negative full scale for 80000000H (@32-bit). The suitable V_{AOUT} is 0 V for 00000000H (@32-bit). The internal switched capacitor filters attenuate the noise generated by the delta-sigma modulator beyond the audio passband. Figure 83 and Figure 84 show examples of external LPF circuit summing the differential outputs by a single op-amp. Figure 85 shows an example of differential output circuit and external LPF circuit with two op-amps. Figure 86 shows an example of external LPF circuit with two op-amps when the MONO bit = "1". A resistor that has 0.1 % or less absolute error is recommended for external LPFs.

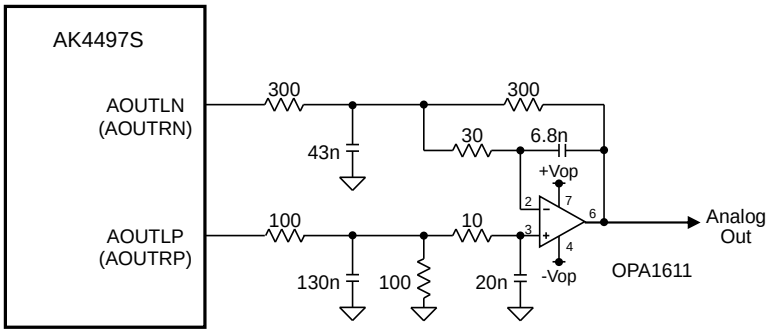


Figure 83. External LPF Circuit Example 1 (fc = 98 kHz(typ.), Q = 0.667(typ.))
(HLOAD pin = “H” or HLOAD bit = “1”)

Table 51. Frequency Response of External LPF Circuit Example 1

Gain (1 kHz, typ.)		0 dB
Frequency Response (ref:1 kHz, typ.)	20 kHz	−0.07 dB
	40 kHz	−0.32 dB
	80 kHz	−2.13 dB

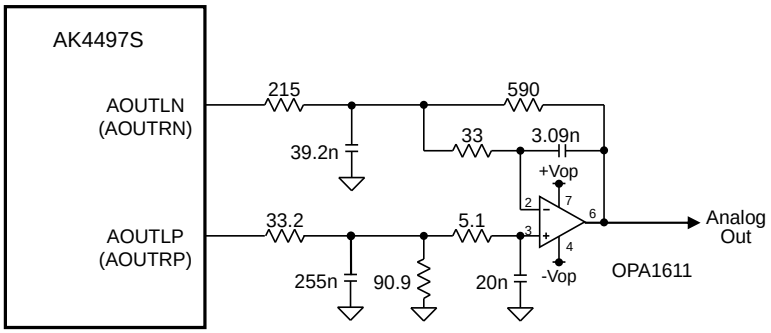


Figure 84. External LPF Circuit Example 2 (fc = 104 kHz(typ.), Q = 0.693(typ.))
(HLOAD pin = “H” or HLOAD bit = “1”)

Table 52. Frequency Response of External LPF Circuit Example 2

Gain(1 kHz ,typ.)		+8.78 dB
Frequency Response (ref:1 kHz, typ.)	20 kHz	−0.02 dB
	40 kHz	−0.15 dB
	80 kHz	−1.46 dB

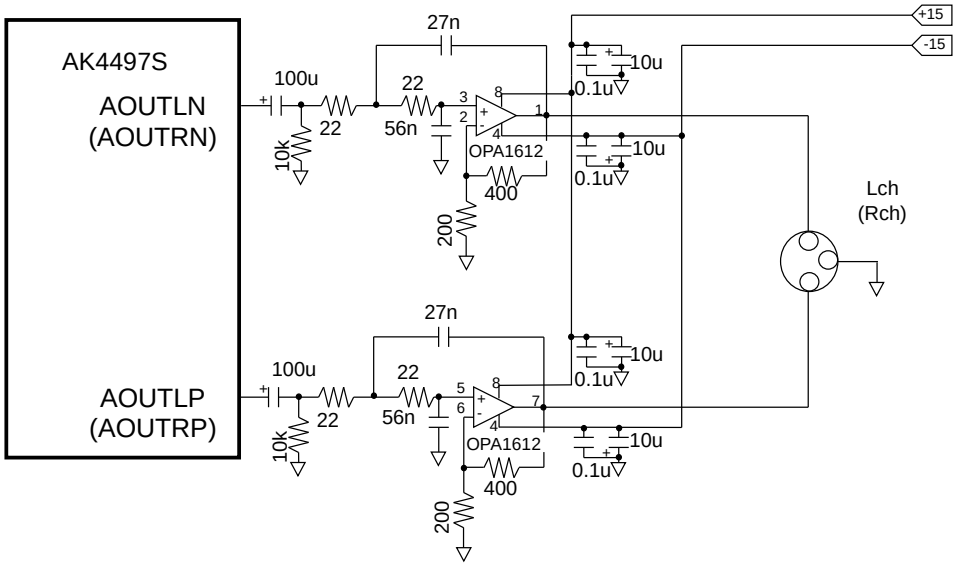


Figure 85. External LPF Circuit Example 3 (fc = 186 kHz(typ.), Q = 0.67(typ.))
(HLOAD pin = “L” or HLOAD bit = “0”)

Table 53. Frequency Response of External LPF Circuit Example 3

Gain(1 kHz, typ.)		+9.54 dB
Frequency	20 kHz	−0.01 dB
Response	40 kHz	−0.06 dB
(ref:1 kHz, typ.)	80 kHz	−0.32 dB

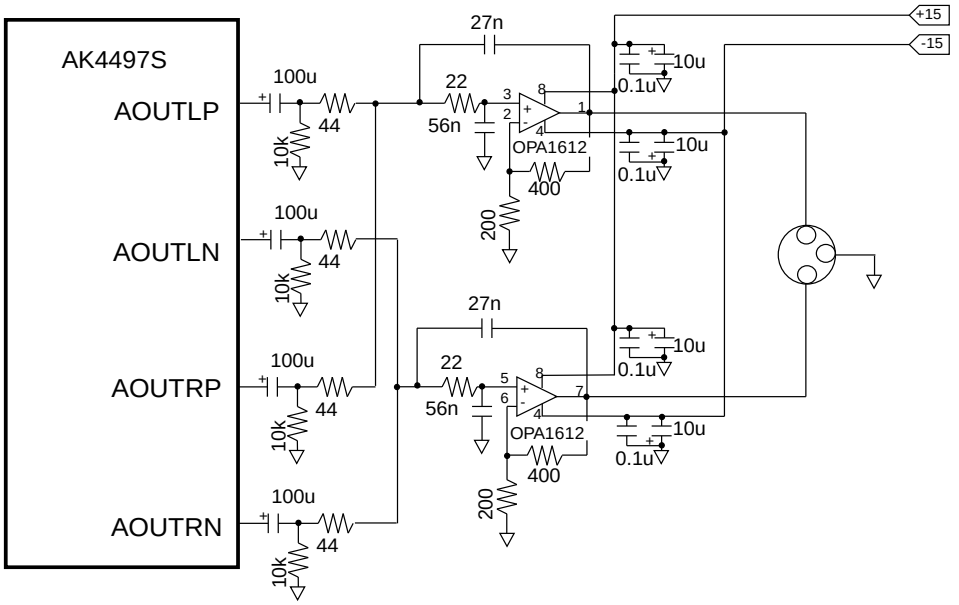
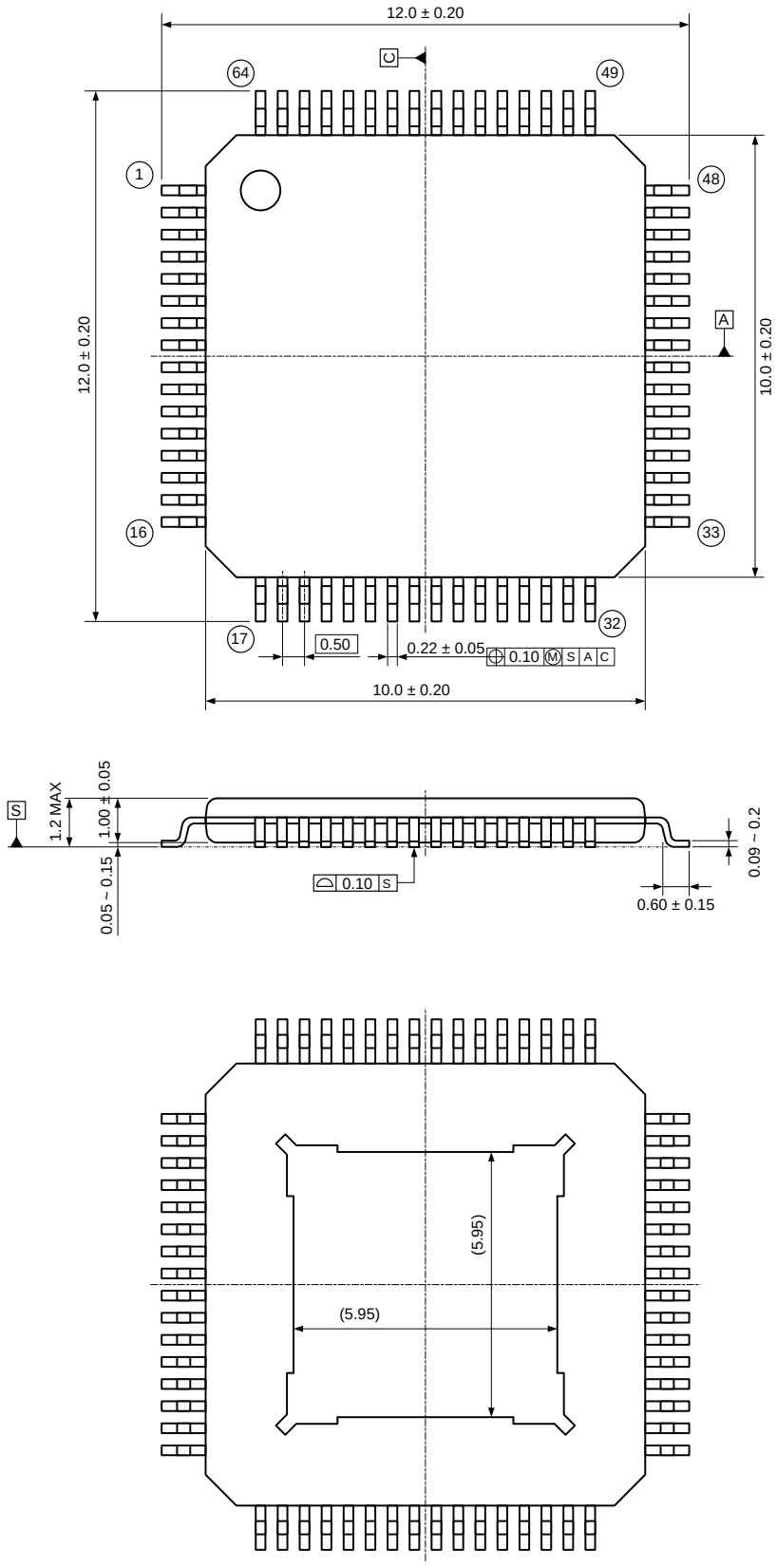


Figure 86. External LPF Circuit Example for mono mode (fc = 186 kHz(typ.), Q = 0.67(typ.))
(HLOAD pin = “L” or HLOAD bit = “0”)

11. Package

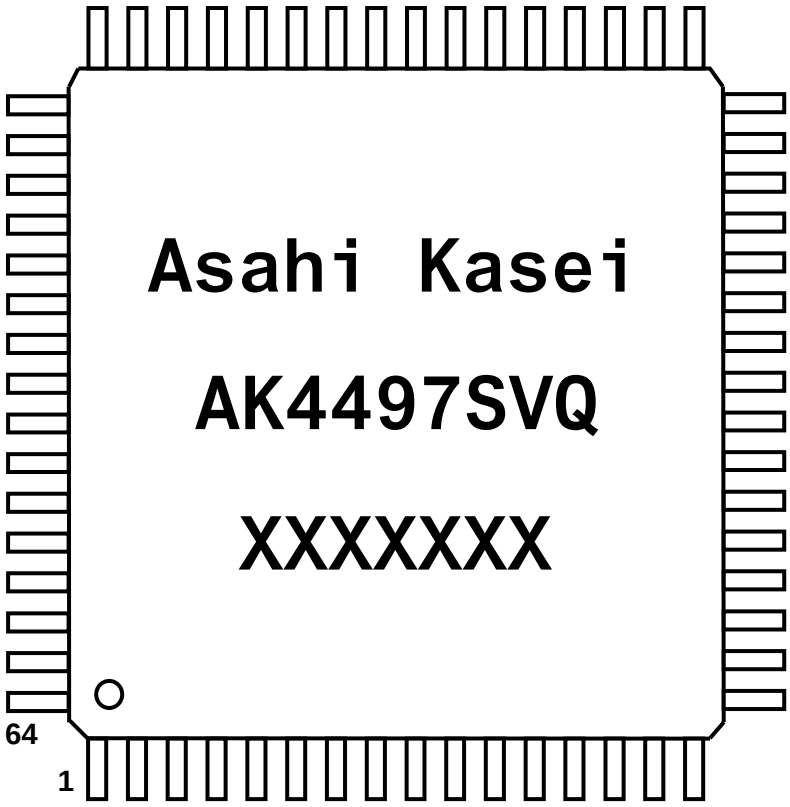
11.1. Outline Dimensions



11.2. Material & Lead Finish

Package molding compound:	Epoxy, Halogen (bromine and chlorine) free
Lead frame material:	EFTEC64
Pin surface treatment:	Solder (Pb free) plate

11.3. Marking



1) Pin #1 indication
2) Date Code: XXXXXXX (7 digits)
3) Marking Code: AK4497SVQ
4) Asahi Kasei company name

12. Ordering Guide

AK4497SVQ	−40 ~ +105°C (Assuming the exposed pad is connected to the printed circuit board) 64-pin TQFP (0.5mm pitch)
AKD4497S	Evaluation Board for AK4497S

13. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
25/04/11	00	First Edition	-	-

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