AsahiKASEI MICRODEVICES

AKD4497S-A

AK4497S Evaluation Board Rev.0

1. General Description

The AKD4497S-A is an evaluation board for the AK4497S (Premium multi-bit 2ch DAC) that supports Network-Audio systems, USB-DAC, Car-Audio systems. It integrates a digital audio interface receiver (DIR) and differential output low pass filters, allowing quick evaluation with digital audio interface.

■ Ordering Guide

AKD4497S-A -- Evaluation Board for the AK4497S
(A USB I/F board for IBM-AT compatible computers and control software are included in this package.)

2. Features

- **32-bit Stereo DAC (AK4497S)**
- **Digital Audio Interface Receiver (AK4118A)**
- **Low Pass Filters (LPF) for Pre-amplifier Outputs**

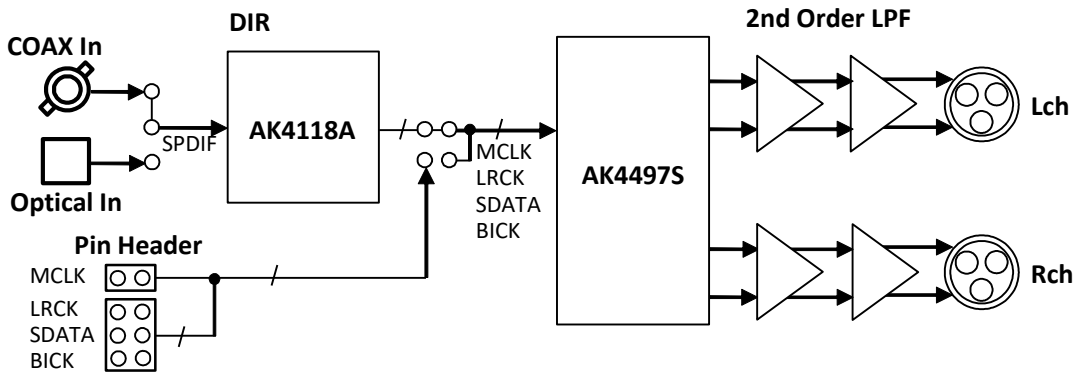


Figure 1. AKD4497S-A Block Diagram (Note 1)

Note 1. Circuit schematics are attached at the end of this document.

3. Board Appearance

■ Appearance Diagram

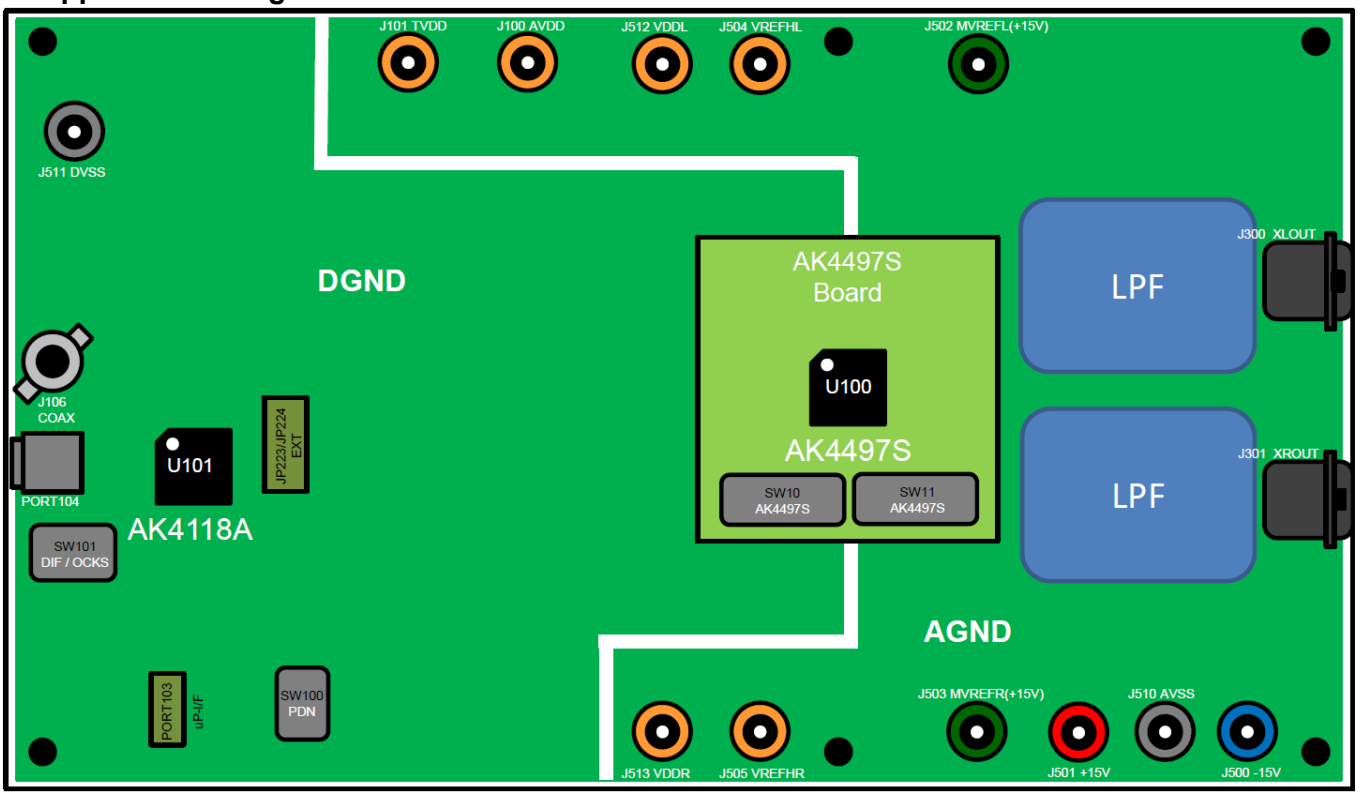


Figure 2. AKD4497S-A Outline View

■ Description

(1) Connectors for Power Supply and GND
J501 +15V/ J500 –15V/ J510 AVSS/ J511 DVSS
J100 AVDD/ J101 TVDD/ J512 VDDL/ J513 VDDR/ J504 VREFHL/ J505 VREFHR
J502 MVREFL(+15V)/ J503 MVREFR(+15V)
Refer to the "■ Power Supply Connections" for details.

(2) SPDIF Input Connectors
J106 COAX, BNC Connector/ PORT104, Optical Connector
Input a SPDIF signal to the AK4118A.

(3) External Clocks and Data Input Connectors
JP223 EXT/ JP224 EXT

(4) AK4497S
U100 (Mounted on sub-board AKD4497-A-SUB-64LTQFP)

(5) LPF Circuits for AK4497S Output
LPF

(6) Connectors for LPF Differential Output
J300 XLOUT/ J301 XLOUT, XLR Connector

(7) AK4118A
U101
The AK4118A is a digital audio interface transceiver. It is used when evaluating AK4497S by SPDIF signal.

(8) I^2C Bus or 3-wire Serial Control Signal Connecting Port
PORT103 µP-I/F, 10-pin Header
Connect the USB I/F board to this port. Refer to the "■ USB I/F board Settings" for details.

(9) DIP Switches for the AK4497S and the AK4118A Pin Settings
Main Board: SW101
Sub Board: SW10/ SW11
Refer to "■ Jumper Pin and DIP Switch Settings" for details.

(10) Toggle Switch for resetting the AK4497S and the AK4118A
SW100 PDN, Toggle Switch
Upside is "H" (Normal Operation) and Downside is "L" (Power down and Reset).

4. Operation Sequence

Please set up the evaluation board in the following order.

1). Power Supply Connectors
2). Clock and Data Input Path Settings
3). Jumper Pin and DIP Switch Settings
4). Power-up

■ Power Supply Connections

With the default jumper settings, the powers required for all devices are generated by regulators on board from the +15V and -15V supplied to J501 and J500. If you are supplying power to AK4497S separately, please refer to Table 2 for power connections and jumper settings.

Table 2. Power Supply Connectors (Note 2)

No.	Name	Voltage	Destination	Note	Default Setting
J501	+15V	+10 to +15V	Regulators, Op-Amps	Power supply to this jack is always needed.	+15V
J500	-15V	-10 to -15V	Op-Amps	Power supply to this jack is always needed.	-15V
J502	MVREFL(+15V)	+10 to +15V	Regulator for VREFHL of AK4497S	These are used when suppling powers to VREFHL/R regulators separately other regulators. Set the JP509 and JP510 jumper pins to “MVREF” side.	Open
J503	MVREFR(+15V)	+10 to +15V	Regulator for VREFHR of AK4497S		Open
J101	TVDD	+1.7 to +3.6V	TVDD of AK4497S	These are used when supplying TVDD, AVDD from external sources without using regulators. Set the JP100 and JP101 jumper pins to “EXT” side.	Open
J100	AVDD	+1.7 to +3.6V	AVDD of AK4497S		Open
J512	VDDL	+4.75 to +5.25V	VDDL of AK4497S	These are used when supplying VDDL/R from external sources without using regulators. Set the JP505 and JP506 jumper pins to “+5V” side.	Open
J513	VDDR	+4.75 to +5.25V	VDDR of AK4497S		Open
J504	VREFHL	+4.75 to +5.25V	VREFHL of AK4497S	These are used when supplying VREFHL/R from external sources without using regulators. Set the JP501 and JP502 jumper pins to “+5V” side.	Open
J505	VREFHR	+4.75 to +5.25V	VREFHR of AK4497S		Open
J510	AVSS	0V	Analog Ground	GND connection to this jack is always needed.	0V
J511	DVSS	0V	Digital Ground	GND connection to this jack is always needed.	0V

Note 2. Each power supply line should be distributed separately from the power supply unit.

■ Clock and Data Input Path Settings

The default setting is for the coaxial SPDIF input shown in (1). When inputting optical SPDIF or external clocks and data, refer to (2) and (3) for jumper settings.

(1) SPDIF (Coaxial) Input < Default >

The J106 (COAX) jack is used in this mode. The DIR (AK4118A) generates MCLK, BICK, LRCK and SDATA from the J106 input data.
Set the JP108 (RX-SEL) jumper pin to 'Up' side (3 pin "BNC"), and set the JP221 (MCLK-DIR) jumper pin to 'short', and set the JP222 (BICK, SDATA, LRCK) jumper pins to 'short', and set the JP102 (MCLK) jumper pin to 'MCLK-1 short and Xtal open and MCLK-2 open'.

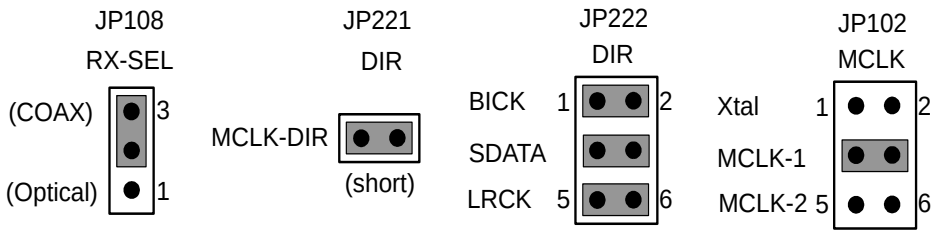


Figure 3. Jumper Pin Settings for Coaxial SPDIF Input

(2) SPDIF (Optical) Input

The PORT104 (Optical) jack is used in this mode. The DIR (AK4118A) generates MCLK, BICK, LRCK and SDATA from the PORT104 input data.
Set the JP108 (RX-SEL) jumper pin to 'Down' side (1 pin "OPT"), and set the JP221 (MCLK-DIR) jumper pin to 'short', and set the JP222 (BICK, SDATA, LRCK) jumper pins to 'short', and set the JP102 (MCLK) jumper pin to 'MCLK-1 short and Xtal open and MCLK-2 open'.

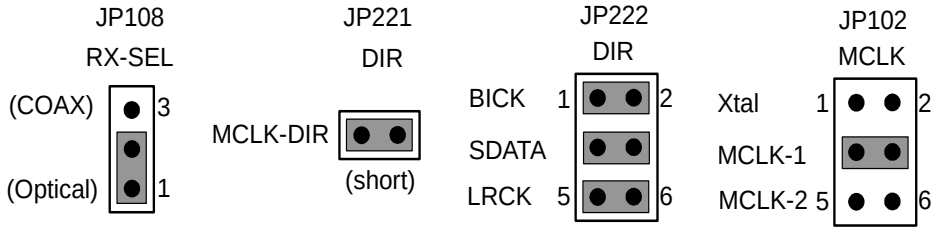


Figure 4. Jumper Pin Settings for Optical SPDIF Input

(3) External Clocks and Data Input

The JP223 and JP224 are used for inputting external clocks and data to AK4497S.
Set the JP221 (DIR: MCLK) and JP222 (DIR: BICK, SDATA, LRCK) jumper pins to 'open'.
Input MCLK to JP223 2 pin, and input BICK, SDATA and LRCK to JR224 2 pin, 4 pin and 6 pin.

External master clock input

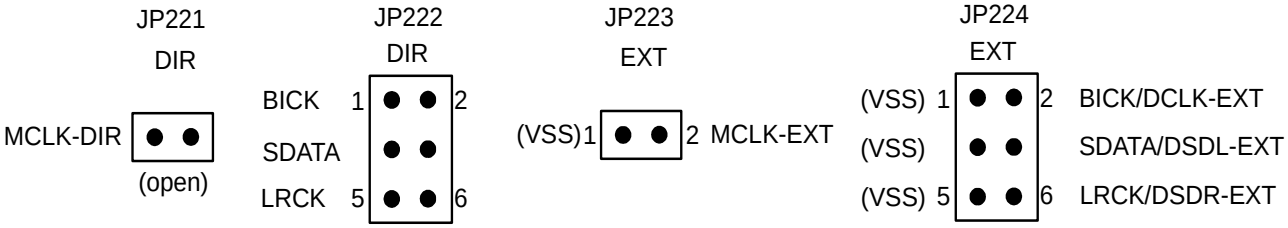
JP223 : MCLK

Signal	Pin No.		Signal
VSS or open	1	2	MCLK

External data and clocks input

JP224 : BICK, SDATA, LRCK

Signal	Pin No.		Signal
VSS or open	1	2	BICK
VSS or open	3	4	SDATA
VSS or open	5	6	LRCK



Note. The silk patterns of signal name for JP223 and JP224 are printed on the opposite side. Please be careful when connecting.

Figure 5. Jumper Pin Settings with External Clocks

When also in DSD or EXDF mode, please input clocks and data from JP223 and JP224. See also Table 3-2-1.

■ Jumper Pin and DIP Switch Settings

Set the jumpers and dip switches according to the powers, clocks and data you use.

(1) Jumper Pin Settings

Table 3-1-1. Jumper Settings for power supply of AK4497S [**Main Board**]

No.	Name	Content	Default Setting
JP100	AVDD	AVDD pin power supply source select EXT: Connector J100 (AVDD) REG(3.3V): 3.3V Regulator T100 REG(1.8V): 1.8V Regulator T104	REG(3.3V)
JP101	TVDD	TVDD pin power supply source select REG(1.8V): 1.8V Regulator T105 REG(3.3V): 3.3V Regulator T101 EXT: Connector J101 (TVDD)	REG(3.3V)
JP501	VREFHL	VREFHL pin power supply source select REG: VREFHL regulator circuit +5V: Connector J504 (VREFHL)	REG
JP502	VREFHR	VREFHR pin power supply source select +5V: Connector J505 (VREFHR) REG: VREFHR regulator circuit	REG
JP509	MVREFL	VREFHL regulator circuit power supply source select MVREF: Connector J502 (MVREFL(+15V)) MVDD+: Connector J501 (+15V)	MVDD+
JP510	MVREFR	VREFHR regulator circuit power supply source select MVDD+: Connector J501 (+15V) MVREF: Connector J503 (MVREFR(+15V))	MVDD+
JP505	VDDL	VDDL pin power supply source select +5V: Connector J512 (VDDL) REG: 5V Regulator T500	REG
JP506	VDDR	VDDR pin power supply source select REG: 5V Regulator T501 +5V: Connector J513 (VDDR)	REG
JP500	VSS-SEL1	Connection between analog VSS pattern and digital VSS pattern. short: Connect open: Detach	short
JP520	VSS-SEL2	Connection between analog VSS pattern and digital VSS pattern. short: Connect open: Detach	short

Table 3-1-2. Jumper Settings for power supplies of AK4497S [**Sub Board**]

No.	Name	Content	Default Setting
JP16	DVDD	DVDD pin power supply source select short: 1.8V Regulator T102 (SW11 “LDOE” = “L”) open: Internal LDO (SW11 “LDOE” = “H”)	short

Table 3-2-1. Jumper Settings for data & clocks [**Main Board**]

No.	Name	Content	Default Setting
JP108	RX-SEL	SPDIF signal input connector select Upside: BNC Connector J106 (COAX) Downside: Optical Connector PORT104	Upside BNC
JP102	MCLK	MCLK pin (AK4497S) clock source select Xtal (1 – 2 short): Cystal Oscillator X400 Output. MCLK-1 (3 – 4 short): DIR (AK4118A) Output or External Clock (JP223 Input). MCLK-2 (5 – 6 short): Not Used	MCLK-1
JP221	DIR	MCLK from DIR (AK4118A) connect to JP102 “MCLK-1” MCLK-DIR short: Connect open: Disconnect	short
JP222	DIR	DATA and Clocks from DIR (AK4118A) connect to AK4497S BICK, SDATA, LRCK short: Connect open: Disconnect	short
JP223	EXT	External MCLK input pin for AK4497S MCLK-EXT: MCLK input pin	open
JP224	EXT	External data and clocks input pins for AK4497S BICK/DCLK-EXT: BICK input pin (PCM mode) BCK input pin (EXDF mode) DCLK1 input pin (DSD mode) SDATA/DSDL-EXT: SDATA input pin (PCM mode) DINL input pin (EXDF mode DSDL1 input pin (DSD mode) LRCK/DSDR-EXT: LRCK input pin (PCM mode) DINR input pin (EXDF mode) DSDR1 input pin (DSD mode)	open

Table 3-3. Jumper Settings for control signal of AK4497S [**Sub Board**]

No.	Name	Content	Default Setting
JP10	PS1	SMUTE/CSN pin input signal select CSN: CSN (Register Control & 3-wire Serial mode) SMUTE: SW10 “SMUTE” (Pin Control mode)	CSN
JP11	PS2	SD/CCLK/SCL pin input signal select CCLK/SCL: CCLK or SCL (Register Control mode) SD: SW10 “SD” (Pin Control mode)	CCLK/SCL
JP12	PS3	SLOW/CDTI/SDA pin input signal select CDTI/SDA: CDTI or SDA (Register Control mode) SLOW: SW10 “SLOW” (Pin Control mode)	CDTI/SDA
JP13	PS4	SSLOW pin setting (Pin Control mode) H: “H” L: “L” WCK input pin (Register Control & EXDF mode)	L
JP14	DZFL	DIF0/DZFL pin setting short: Connected to SW10 “DIF0” (Pin Control mode) open: DZFL can be monitored on this pin. (Register Control mode)	open
JP15	DZFR	DIF1/DZFR pin setting short: Connected to SW10 “DIF1” (Pin Control mode) open: DZFR can be monitored on this pin.(Register Control mode)	open
JP17	TDMO-O	TDMO output data monitor pin TDM output data is monitored on this pin.	open

(2) DIP Switch Setting

Upside is ON (“H”), and Downside is OFF (“L”).

AK4118A Settings: Main Board

Set the audio interface format and MCLK frequency that the AK4118A outputs to the AK4497.

Table 4-1. SW101 Functions (AK4118A)

No.	Name	ON (“H”)	OFF (“L”)	Default
1	DIF2	Audio I/F Format (AK4118A Output) Refer to **Table 4-1-1.**		H
2	DIF1			L
3	DIF0			L
4	OCKS1	Master Clock Frequency (AK4118A Output) Refer to **Table 4-1-2.**		L
5	OCKS0			L

SW101 Setting Tables

Table 4-1-1. Audio I/F Format (AK4118A Output)

DIF2	DIF1	DIF0	SDTO	LRCK		BICK		
L	L	L	16bit Right justified	H/L	O	64fs	O	
L	L	H	18bit Right justified	H/L	O	64fs	O	
L	H	L	20bit Right justified	H/L	O	64fs	O	
L	H	H	24bit Right justified	H/L	O	64fs	O	
H	L	L	24bit Left justified	H/L	O	64fs	O	< Default >
H	L	H	24bit I2S	L/H	O	64fs	O	
H	H	L	24bit Left justified	H/L	I	64-128fs	I	
H	H	H	24bit I2S	L/H	I	64-128fs	I	

Table 4-1-2. Master Clock Frequency (AK4118A Output)

OCKS1	OCKS0	MCKO1	Maximum fs	
L	L	256fs	96 kHz	< Default >
L	H	256fs	96 kHz	
H	L	512fs	48 kHz	
H	H	128fs	192 kHz	

AK4497S Settings : Sub Board

SW10, SW11 and JP13 are used to set the configuration pins of the AK4497S.

Register Control mode (SW10 “PSN” = ”L”)

The JP10, JP11 and JP12 must be set for Register Control mode side.

Table 4-2-1. SW10 Setting (Register Control mode)

No.	Name	ON (“H”)	OFF (“L”)	Default
1	SMUTE	Invalid		L
2	SD	Invalid		H
3	SLOW	Invalid		L
4	(DZFL)	Invalid, JP14 must be open.		L
5	(DZFR)	Invalid, JP15 must be open.		H
6	CAD0	CAD0 pin= “H”	CAD0 pin= “L”	L
7	PSN	Pin Control mode	Register Control mode	L
8	DEM0/DSDL	Invalid		H
9	GAIN/DSDR	Invalid		L
10	CAD1	CAD1 pin= “H”	CAD1 pin= “L”	L

Table 4-2-2. SW11 Setting (Register Control mode)

No.	Name	ON (“H”)	OFF (“L”)	Default
1	LDOE	LDO “ON”	LDO “OFF”	L
2	TDM0/DCLK	Invalid		L
3	TDM1	Invalid		L
4	DCHAIN	Invalid		L
5	INVR	Invalid		L
6	TESTE	Test mode	Normal Operation	L
7	NC	-		L
8	NC	-		L
9	NC	-		L
10	NC	-		L

Pin Control mode (SW10 “PSN” = ”H”)

The JP10, JP11 and JP12 must be set for Pin Control mode side.

Table 4-2-3. SW10 Setting (Pin Control mode)

No.	Name	ON (“H”)	OFF (“L”)	Default
1	SMUTE	Mute “ON”	Mute “OFF”	L
2	SD	Digital Filter Setting: Refer to Table 4-2-3-1. (SSLOW is set by JP13)		H
3	SLOW			L
4	DIF0	Audio I/F Format: Refer to Table 4-2-3-2.		L
5	DIF1			H
6	DIF2			L
7	PSN	Pin Control mode	Register Control mode	(set H)
8	DEM0	De-emphasis “ON” fs = 44.1kHz	De-emphasis “OFF”	H
9	GAIN	Output Level = 2.8Vpp	Output Level = 3.75Vpp	L
10	ACKS	Auto Setting mode	Manual Setting mode	L

Table 4-2-4. SW11 Setting (Pin Control mode)

No.	Name	ON (“H”)	OFF (“L”)	Default
1	LDOE	LDO “ON”	LDO “OFF”	L
2	TDM0	Audio I/F Format. :Refer to Table 4-2-4-1.		L
3	TDM1			L
4	DCHAIN	Daisy Chain mode	Normal mode	L
5	INVR	Rch Signal Invert	Normal	L
6	TESTE	Test mode	Normal mode	L
7	NC	-		L
8	NC	-		L
9	NC	-		L
10	NC	-		L

SW10, SW11 Setting Tables in Pin Control mode

Table 4-2-3-1. Digital Filter Select of the AK4497S

SSLOW JP13	SD	SLOW	Mode	
L	L	L	Sharp roll-off filter	
L	L	H	Slow roll-off filter	
L	H	L	Short delay sharp roll-off filter	< Default >
L	H	H	Short delay slow roll-off filter	
H	L	L	Super Slow roll-off filter	
H	L	H	Super Slow roll-off filter	
H	H	L	Low dispersion Shot Delay filter	
H	H	H	Reserved	

Table 4-2-3-2. Audio I/F Format Select of the AK4497S

DIF2	DIF1	DIF0	Input Format	BICK	
L	L	L	16bit LSB justified	≥ 32fs	
L	L	H	20bit LSB justified	≥ 48fs	
L	H	L	24bit MSB justified	≥ 48fs	< Default >
L	H	H	24bit I^2S Compatible	≥ 48fs	
H	L	L	24bit LSB justified	≥ 48fs	
H	L	H	32bit LSB justified	≥ 64fs	
H	H	L	32bit MSB justified	≥ 64fs	
H	H	H	32bit I^2 Compatible	≥ 64fs	

Table 4-2-3-3. De-emphasis Control Enable of the AK4497S

DEM0	De-emphasis Mode	
L	ON (fs = 44.1 kHz)	
H	OFF	< Default >

Table 4-2-4-1. Audio I/F Format Select of the AK4497S

TDM1	TDM0	Input Format Mode	
L	L	Normal Mode	< Default >
L	H	TDM128 Mode	
H	L	TDM256 Mode	
H	H	TDM512 Mode	

Table 4-2-4-2. Output Phase Inversion Enable of the AK4497S

INVR	Lch Out	Rch Out	
L	Lch In	Rch In	< Default >
H	Lch In	Rch In Invert	

■ Zero-ohm Resistors Settings: Main Board

Table 4-2-3-1. Zero-ohm Resistors Setting

Resistor	Sub Board Signal	Setting for Sub Board	Default
R1001 R1002	HLOAD/I2C	R1001=short, R1002=open: HLOAD/I2C="H" R1001=open, R1002=short: HLOAD/I2C="L"	HLOAD/I2C=H (R1001=short,R1002=open)

Table 4-2-3-2. HLOAD/I2C Setting (AK4497S)

Control Mode	Name	"H"	"L"
Pin Control mode	HLOAD	Heavy Load mode	Normal Load mode
Register Control mode	I2C	I^2C-Bus Control Mode	3-wire Serial Control Mode

■ Power-up

Before powering on the evaluation board, use toggle switch SW100 to fix the PDN pins of the AK4497S and AK4118A to “L”.

No.	Name	Content	Default Setting
SW100	PDN	Power down and reset AK4497S and AK4118A. H: Normal Operation L: Power down and Reset	-

Turn on the power supplies while PDN = “L”. When the AK4497S is powered directly from an external source, TVDD must be powered up before or at the same time as DVDD. There are no other restrictions on power-up order.

(1) Pin Control mode

After powering on, input the SPDIF signal (or external clocks and data).
Next, set SW100 to "H" to release the power down and the AK4497S will start operating.

(2) Register control mode

After powering on, connect the USB-I/F board to the PC with a USB cable and connect the flat cable to the 10-pin header PORT103 on the evaluation board. Then Input the SPDIF signal (or external clocks and data). Set the SW100 to "H" to release the power down.

Open the control software “ak4497S.exe”.
After setting the necessary registers, reset the internal circuit once by setting the RSTN bit to "0". Then, release the reset by setting RSTN bit to "1", and the AK4497S will start operating.

The USB-I/F board and the control software are packed with the evaluation board.

5. Example of evaluation

Below is an example of usage with the board's default settings.

■ Default Setting of the evaluation board

Power Supply Connecters:	+15V, -15V (J501, J500)
Evaluation Mode:	DIR (COAX) Input
Clocks (AK4118A Output):	fs=44.1kHz, MCLK=256fs, BICK=64fs
Data Format (AK4118A Output):	24-bit Left Justified
Control Mode:	I²C Control mode, Chip Address = 00b

■ Start-up

1: Set the toggle switch SW100 to “L”.
2: Power up the +15V and -15V.
3. Connect the USB-I/F board
4. Input SPDIF signal
5: Set the toggle switch SW100 to “H”.
6: Open the control soft “ak4497s.exe”
  6-1: Set “Control I/F” area: I2C, CAD00
  6-2: Click [InitPort] button and [WriteDefault] button.
  6-3: Script Tab -> [Refer] -> Select “ak4497s-defaultset.txt” -> [Open]
  6-4: Reset and reset release by RSTN bit

  Note. The “ak4497s-defaultset.txt” is packed with CR-ROM the evaluation board.

Register Setting after load “ak4497s-default.txt”

00H-10H	11H-15H	Address	Example Indication // Button UP is "L" or "0" // Button DOWN is "H" or "1" //Blanks are invalid.							
00H	0DH	ACKS	EXDF	ECS	AFSD	DIF2	DIF1	DIF0	RSTN
01H	22H	DZFE	DZFM	SD	DFS1	DFS0	DEM1	DEM0	SMUTE
02H	00H	DP	ADP	DCKS	DCKB	MONO	DZFB	SELLR	SLOW
03H	FFH	ATTL7	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
04H	FFH	ATTR7	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0
05H	00H	INVL	INVR	---	---	---	---	DFS2	SSLOW
06H	00H	DDM	DML	DMR	DDMOE	DDMT1	DDMT0	DSDD	DSDSEL0
07H	01H	MSTBN	---	---	---	GC2	GC1	GC0	SYNCE
08H	00H	---	---	---	---	HLOAD	SC2	SC1	SC0
09H	00H	---	ERRMSK	ZEROMSK	DSDD2	---	DSDPATH	DSDF	DSDSEL1
0AH	04H	TDM1	TDM0	SDS1	SDS2	---	STBYN	---	---
0BH	00H	ATS1	ATS0	---	SDS0	---	---	DCHAIN	THDE
0CH	00H	DGERRINT	DGSELOVF	DGCLP1	DGCLP0	DGSYNCER	DGSYNCC	DGSYNCW'	DGSYNCW(
0DH	00H	---	---	---	---	---	CRAMR	CRAMW	CRAMCLR
0EH	00H	FIRT7	FIRT6	FIRT5	FIRT4	FIRT3	FIRT2	FIRT1	FIRT0
0FH	00H	FIRC23	FIRC22	FIRC21	FIRC20	FIRC19	FIRC18	FIRC17	FIRC16
10H	00H	FIRC15	FIRC14	FIRC13	FIRC12	FIRC11	FIRC10	FIRC9	FIRC8

00H-10H	11H-15H	Address	Example Indication // Button UP is "L" or "0" // Button DOWN is "H" or "1" //Blanks are invalid.							
11H	00H	FIRC7	FIRC6	FIRC5	FIRC4	FIRC3	FIRC2	FIRC1	FIRC0
12H	00H	RFIRC23	RFIRC22	RFIRC21	RFIRC20	RFIRC19	RFIRC18	RFIRC17	RFIRC16
13H	00H	RFIRC15	RFIRC14	RFIRC13	RFIRC12	RFIRC11	RFIRC10	RFIRC9	RFIRC8
14H	00H	RFIRC7	RFIRC6	RFIRC5	RFIRC4	RFIRC3	RFIRC2	RFIRC1	RFIRC0
15H	00H	ADPE	ADPT1	ADPT0	---	---	ADFS2	ADFS1	ADFS0

Main contents of the default register settings

Conversion Mode:	PCM mode
Data Format:	32-bit Left Justified, BICK ≥ 64fs
Clocks:	Normal Speed mode, MCLK = 256fs, 384fs, 512fs or 768fs

■ USB I/F board Settings

The AKD4497S-A (for the AK4497S) should be connected to a PC (IBM-AT compatible) via a USB I/F board (AKDUSBIF-B) included in this package. The USB I/F board is connected to a PC with a USB cable and the AKD4497S-A with a 10-pin flat cable. (Note.3, Note.4)

Note 3. The AKD4497S-A accepts only one AKDUSBIF-B at one time. It does not operate if two or more AKDUSBIF-Bs are connected.
Note 4. Connect the 10pin Flat Cable as the red line of the cable is connected to the 1 pin of the 10pin Header (PORT103) on the board.

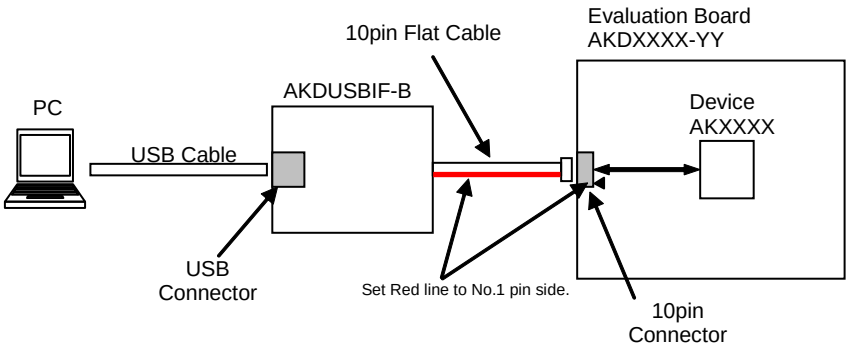


Figure 10. AKDUSBIF-B Connection

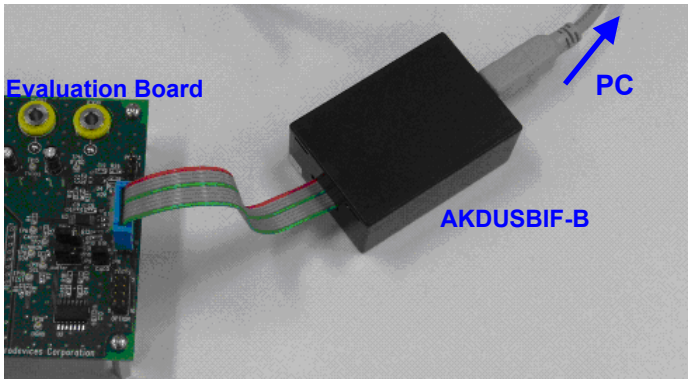


Figure 11. AKDUSBIF-B

Register Control Mode settings : Selected Position

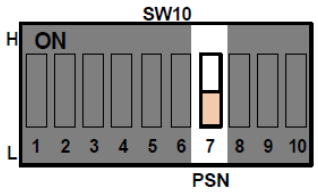
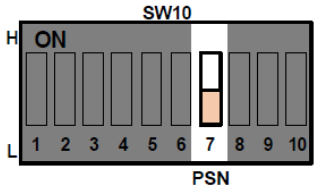
Register Control Mode	Sub-board (AK4497S) (SW10-No.7: PSN)	Main Board (AK4497S) (R1001,R1002 : I2C)	Control Software (Control I/F)
3-wire Serial	 PSN = L	R1001=open R1002=short I2C = L	
I²C-Bus	 PSN = L	R1001=short R1002=open I2C = H	

Table 6-1. Register Control Mode setting

When using this evaluation board in Register Control mode, settings of the CAD1 pin and the CAD0 pin on the board must match the chip address settings of the control software.

Chip Address settings

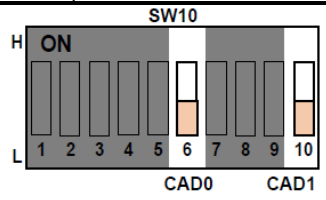
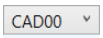
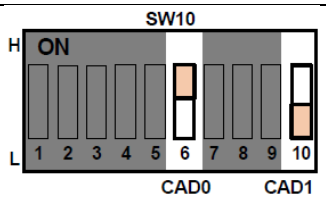
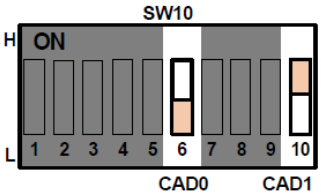
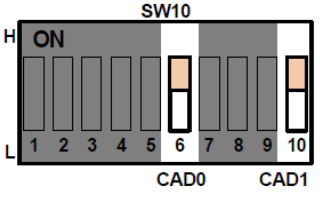
Chip Address	Sub-board (AK4497S) (SW10-No.10: CAD1, -No.6: CAD0)	Control Software (Chip Address)
“00”	 CAD1-0 = LL	
“01”	 CAD1-0 = LH	
“10”	 CAD1-0 = HL	
“11”	 CAD1-0 = HH	

Table 6-2. “Chip Address” setting

Set up the jumper pins.

JP10 = CSN short, JP11 = CCLK/SCL short, JP12 = CDTI/SDA short
JP13 = L short, JP14 = open, JP15 = open

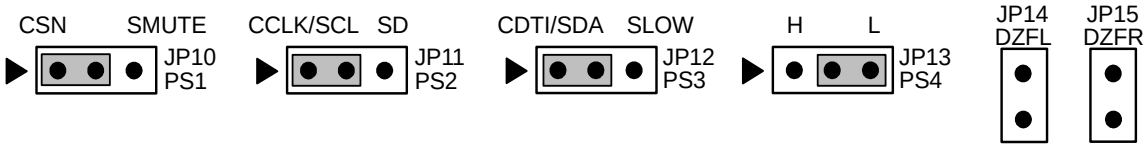


Figure 12. Jumper pin setting

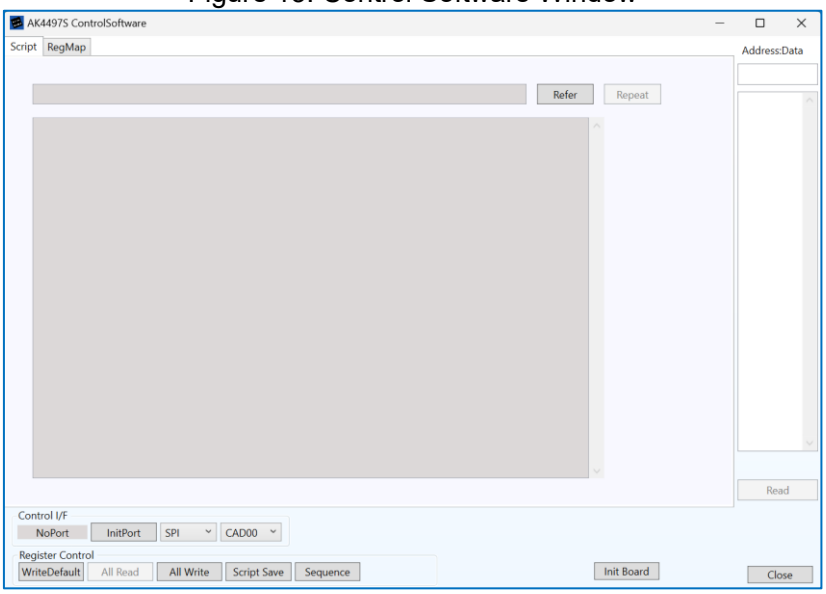
6. Control Software Manual

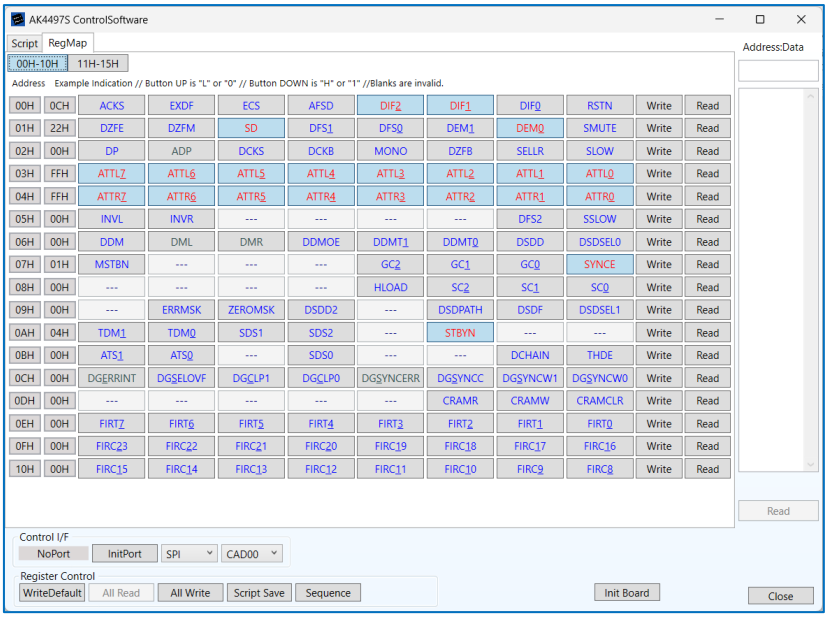
■ Evaluation Board and Control Software Settings

1. Set up the evaluation board as needed, according to the previous terms.
2. Connect the evaluation board to a PC with USB I/F board.
3. USB control is recognized as HID (Human Interface Device) on PC. When it is not recognized properly, please reconnect the evaluation board to PC.
4. Insert the CD-ROM labeled “AKD4497S-A Evaluation Kit” into the CD-ROM drive.
5. Access the CD-ROM drive and double-click the icon “ak4497s.exe” to open the control software.
6. Begin evaluation by following the procedure below.

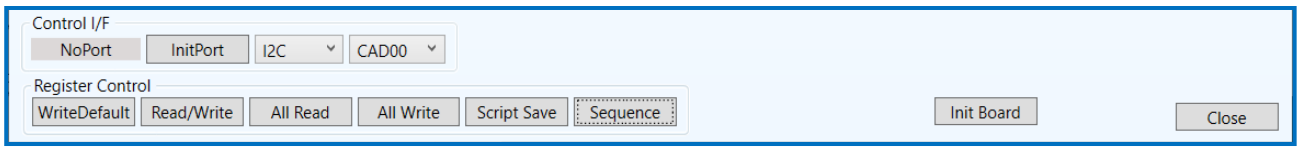
[Supported OS]
Windows 7 (32bit) / Windows 10 (64bit) / Windows 11 (64bit)

Figure 13. Control Software Window





■ Operation Overview



Frequently used buttons, such as the register initializing button “Write Default”, are located outside of the switching tab window. Refer to the “■ Dialog Box” section for details of each dialog box setting.

1.[Init Port]: Reset the USB port.
Click this button after the control software starts up.

2.[SPI / I2C]: Select up interface of the AK4497S.
This setting can be changed when the PDN pin = “L”.

3.[CAD00 / CAD01 / CAD10 / CAD11]: Select the CAD pin settings.
This setting can be changed when the PDN pin = “L”.

4.[Write Default]: Initialize all registers of the AK4497S.

5.[All Read]: Executes read commands for all registers displayed. (Note 5)

6.[All Write]: Executes write commands for all registers displayed.

7.[Script Save]: Select a file and save all settings of this software.
The saved file can be used as a script.

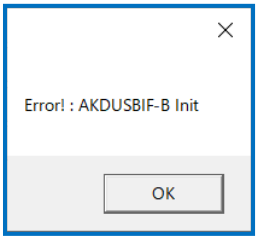
8.[Sequence]: [Sequence] dialog box pops up.

9.[Init Board]: Reset the USB port and writing the default settings.

10.[Close]: Quit the control software.

Note 5. The [All Read] button is only valid when the interface mode for register control is in I^2C bus mode.

If the communication check fails when starting the control software, the following message will be displayed. Click "OK" and check the cable connection.



■ Tab Functions

1. [RegMap] Tab: Register Map

This tab is for register read and write.

Each bit on the register map is a push-button switch. The button is blue when down and gray when up.
Button Down indicates “1” and the bit name is shown in red (when read-only the name is shown in dark red).
Button Up indicates “0” and the bit name is shown in blue (when read-only the name is shown in gray)
Each time the button is clicked, the value toggles between “0” and “1”, and the changed value is written to the AK4497S register.

The registers which are not defined on the datasheet are indicated as “---”.

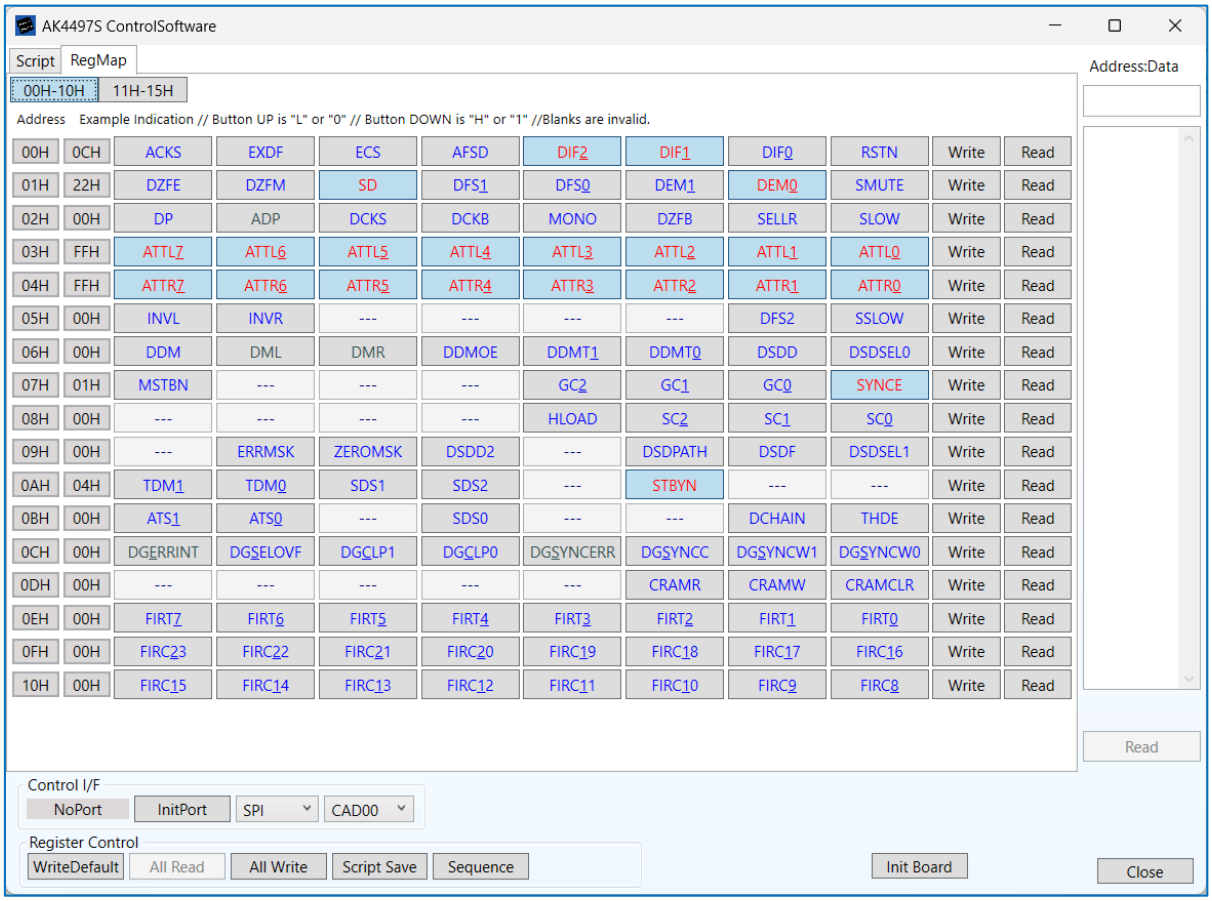


Figure 14-1. RegMap Window

[Write] button: Data Write Dialog

Use the [Write] button located on the right of the corresponding address in the register map when changing two or more bits on the same address simultaneously.

Click the [Write] button to pop-up the dialog box shown below.

When the checkbox is checked, the write data will become “1”. When the checkbox is not checked, the write data will become “0”. Click [OK] to write the set data to the registers. Clicking [Cancel] will close the dialog box without writing to the register.

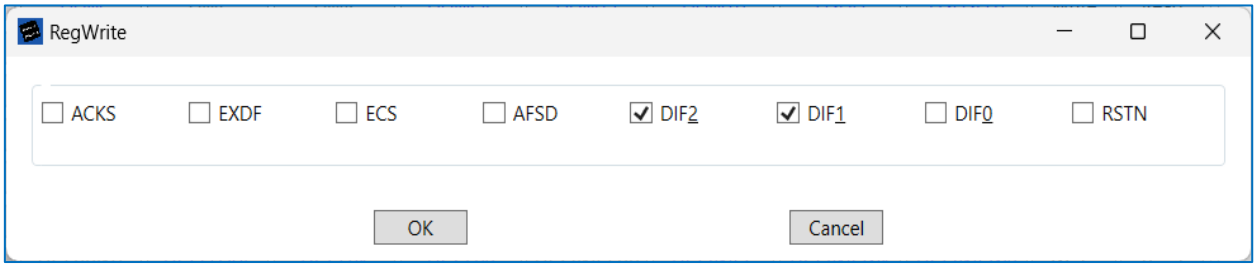


Figure 14-2. Register Set Window

[Read] button: Data Read (Only in I^2C-bus Control Mode)

Click the [Read] button located on the right of each address to execute a register read.
The current register value will be displayed in the register map window as well as in the upper right hand ”Address: Data” box.

2. [Script] Tab : Script Function

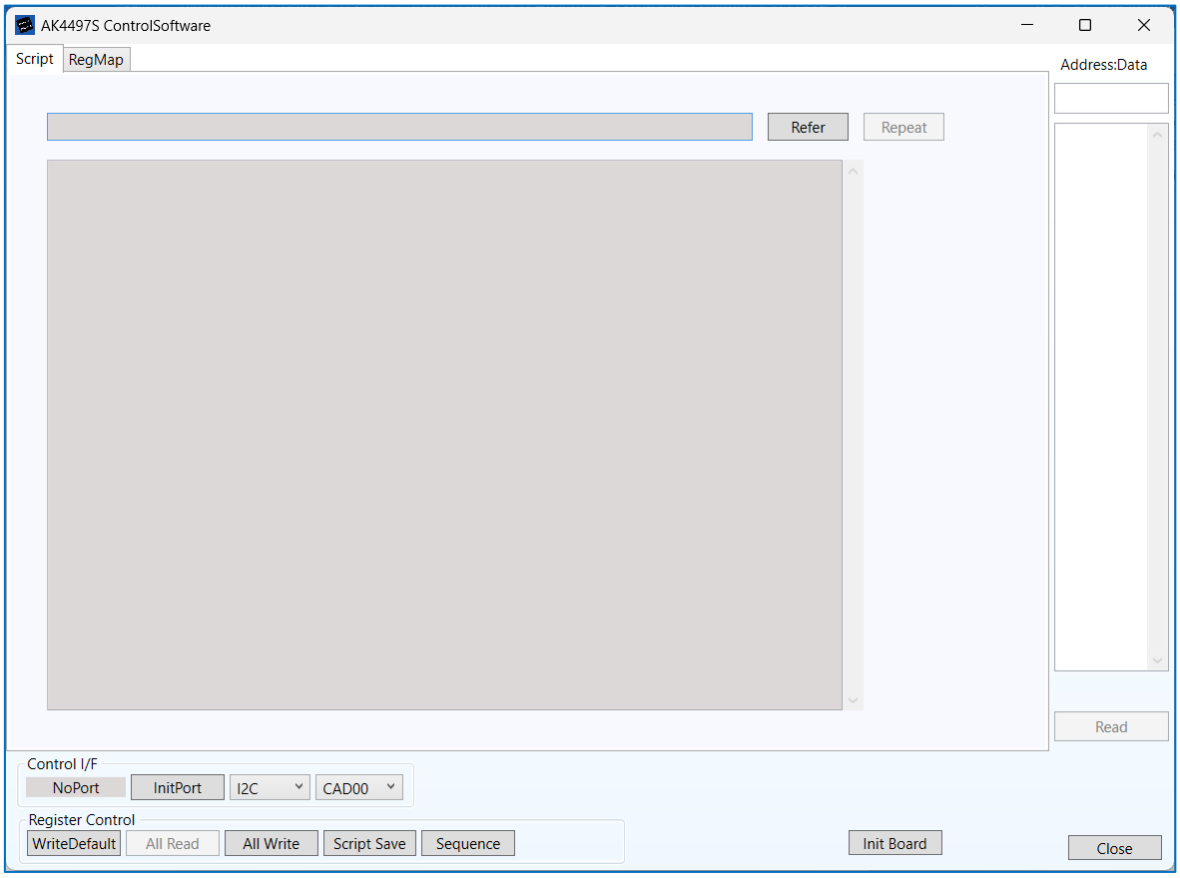


Figure 15. Window of [Script]

[Refer] : Select a script file. The script written on the file will be executed automatically.
[Repeat] : The selected script file will be executed once again.

■ Dialog Box

1. [Sequence]: Sequence Dialog Box

Click the [Sequence] button in the main window for Sequence dialog box.
Register sequence may be set and executed.

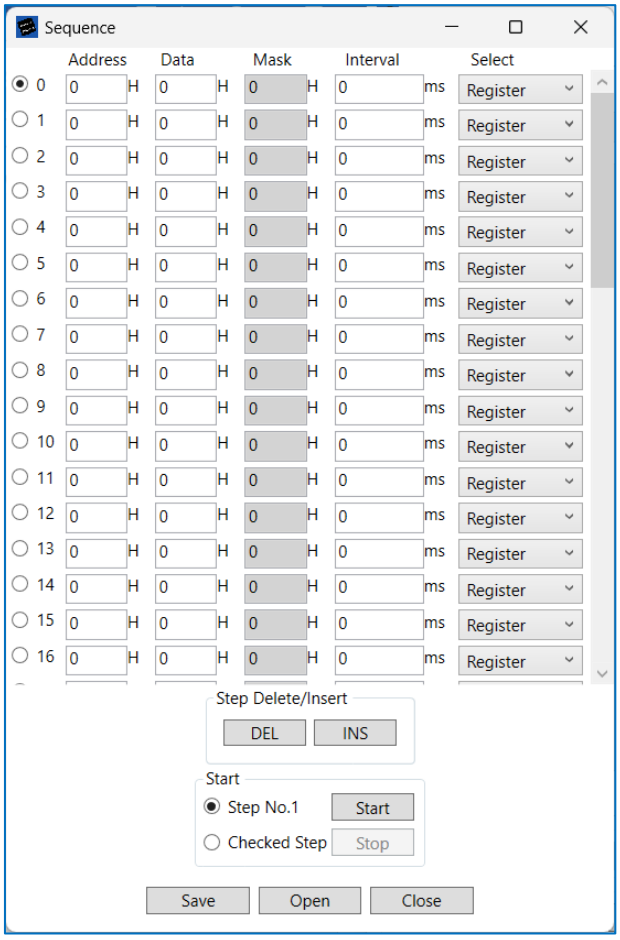


Figure 16. [Sequence] Window

~ Sequence Setting ~

Set register sequence according to the following process.

1. Select a command

   Use [Select] combo box to choose commands.
   Corresponding input boxes will be valid.

<Combo Box>
- No_use: Not using this address
- Register: Register write
- Reg(Mask): Register write (Masked)
- Interval: Take an interval
- Stop: Pause the sequence
- End: End the sequence

2. Input Sequence

[Address]: Data Address
[Data]: Write Data
[Mask]: Mask
This value “ANDed” with the write data becomes the input data.
When Mask = 0x00, current setting is hold.
When Mask = 0xFF, the 8bit data which is set in the [Data] box is written.
When Mask = 0x0F, lower 4bit data which is set in the [Data] box is written.
Upper 4bit is hold to current setting.
[Interval]: Interval Time

Valid boxes for each process command are shown below.

- No_use : None
- Register : [Address], [Data], [Interval]
- Reg(Mask) : [Address], [Data], [Mask], [Interval]
- Interval : [Interval]
- Stop : None
- End : None

~ Control Buttons ~

Functions of Control Buttons are shown below.

[Start] button : Execute the sequence.
[Stop] button : Pause the sequence.
[Save] button : Save sequence settings as a file. The file name is “*.aks”.
[Open] button : Open a sequence setting file “*.aks”.
[Close] button : Close the dialog box and finishes the process.

Start Sequence: [Start] Functions

[Step No.1] check box : Start at number “0” in the sequence.
[Checked Step] check box : Start from checked number in the sequence.

7. Revision History

Date (y/m/d)	Manual Revision	Board Revision	Reason	Page	Contents
24/11/14	KM139100	0	First Edition	-	

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8. Measurement Results

[Measurement condition]

- Measurement unit : Audio Precision APX555 audio analyzer (APX555)
- MCLK : 256fs (44.1 kHz), 256fs (96kHz), 128fs (192kHz)
- BICK : 64fs
- fs (ACKS bit) : 44.1kHz (ACKS=0), 96kHz (ACKS=1), 192kHz (ACKS=1)
- Bit : 24bit
- Power Supply for AK4493S: AVDD=3.3V, TVDD=3.3V, DVDD=1.8V
  VDDL/R=5V, VREFHL/R=5V
- Pass : DIR → AK4493S → Cannon Connector
- Interface : Internal DIR (44.1 kHz / 96kHz / 192kHz)
- Temperature : Room Temperature
- Operational Amplifiers : OPA1612

fs=44.1kHz : ACKS bit =0

Parameter	Input signal	Measurement filter	Results		
			Lch	/	Rch
THD+N	1kHz, 0dB	20kHz LPF	116.3 dB	/	117.2 dB
DR	1kHz, -60dB	20kHz LPF	67.0 dB	/	67.0 dB
		20kHz LPF A-weighted	129.0 dB	/	129.0 dB
S/N	“0” data	20kHz LPF A-weighted	129.0 dB	/	129.0 dB

fs=96kHz : ACKS bit =1

Parameter	Input signal	Measurement filter	Results		
			Lch	/	Rch
THD+N	1kHz, 0dB	40kHz LPF	115.3 dB	/	116.1 dB
DR	1kHz, -60dB	40kHz LPF	63.9 dB	/	64.1 dB
		40kHz LPF A-weighted	129.0 dB	/	129.0 dB
S/N	“0” data	40kHz LPF A-weighted	129.0 dB	/	129.0 dB

fs=192kHz : ACKS bit =1

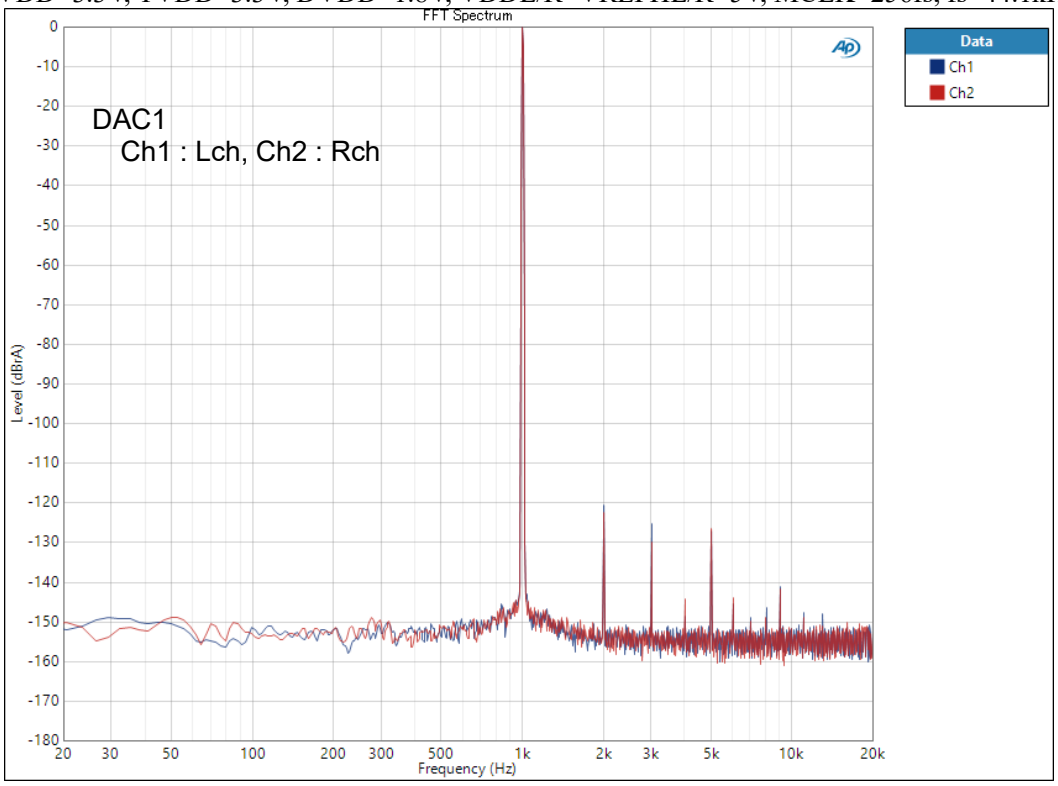
Parameter	Input signal	Measurement filter	Results		
			Lch	/	Rch
THD+N	1kHz, 0dB	80kHz LPF	115.3 dB	/	115.9 dB
DR	1kHz, -60dB	80kHz LPF	63.8 dB	/	64.1 dB
		80kHz LPF A-weighted	129.0 dB	/	129.1 dB
S/N	“0” data	80kHz LPF A-weighted	129.0 dB	/	129.1 dB

[Plots]

fs = 44.1 kHz

AK4497S FFT (0dBFS Input)

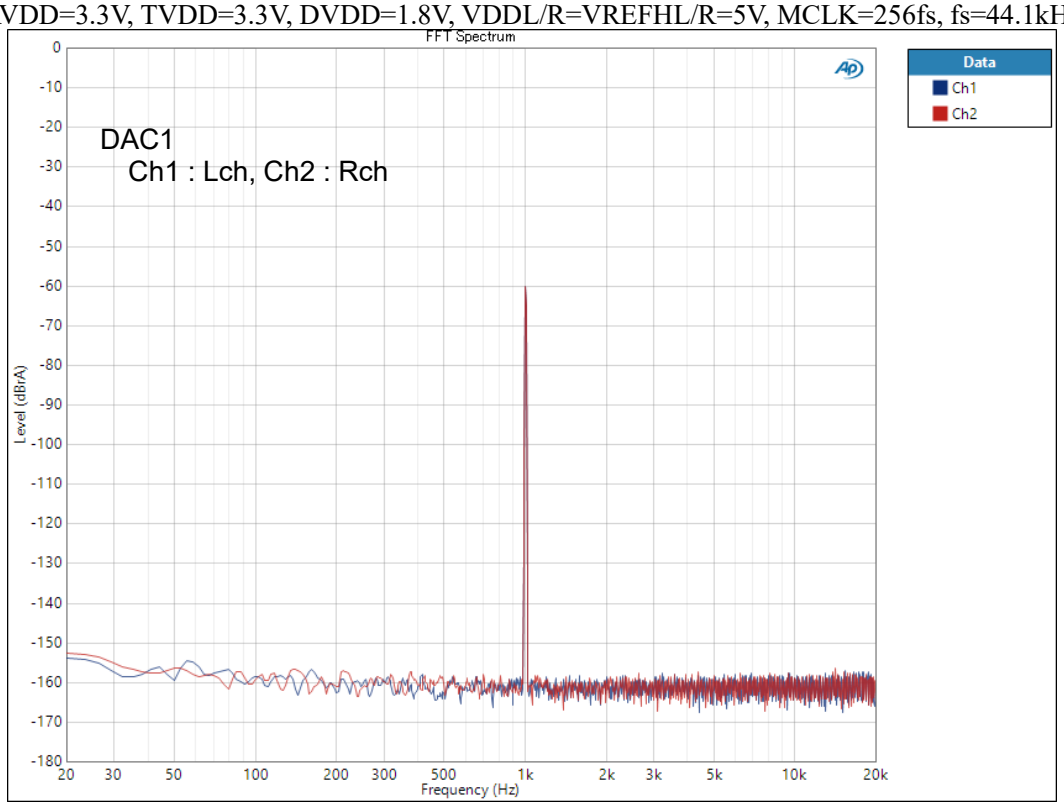
AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=44.1kHz



Plot Figure A-1. FFT (0dBFS Input)

AK4497S FFT (-60dBFS Input)

AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=44.1kHz

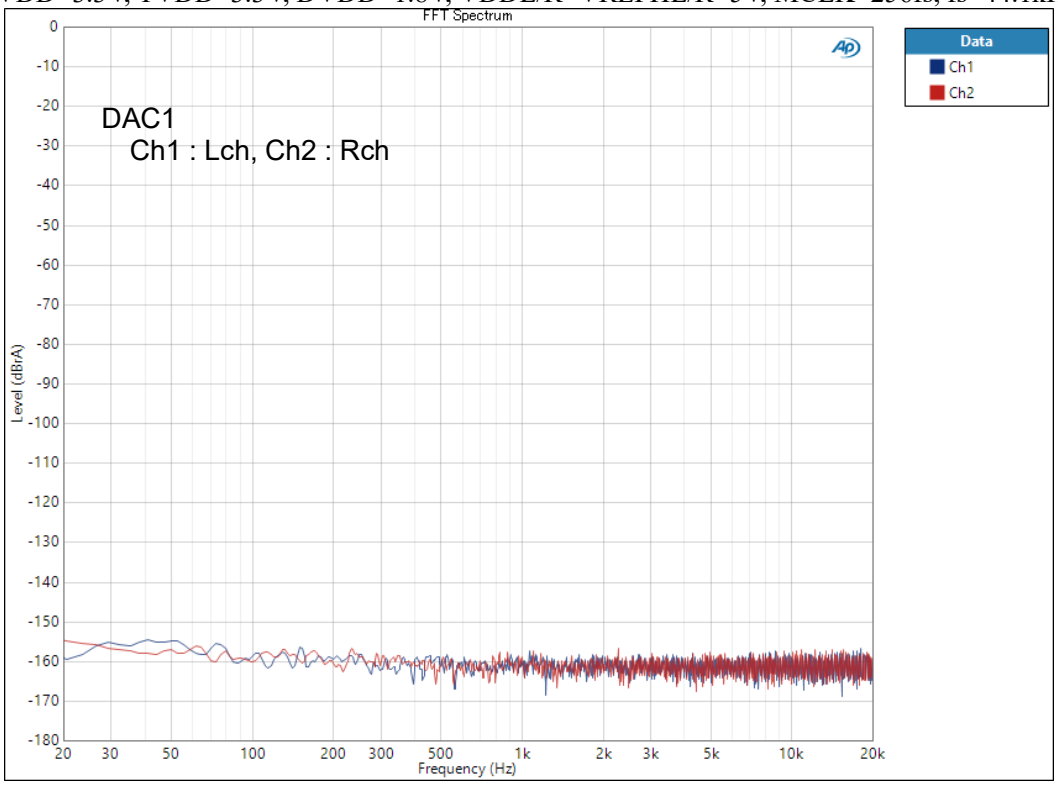


Plot Figure A-2. FFT (-60dBFS Input)

fs = 44.1 kHz

AK4497S FFT (“0” data Input)

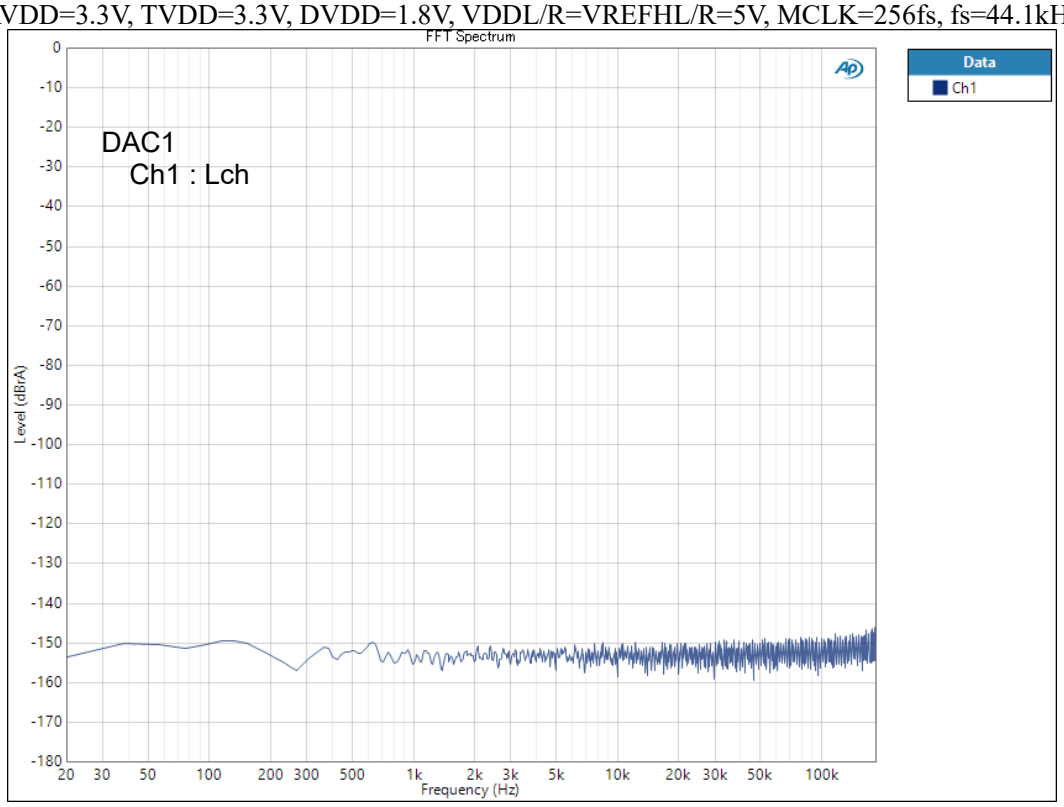
AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=44.1kHz



Plot Figure A-3. FFT (“0” data Input)

AK4497S Out of Band Noise (“0” data Input)

AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=44.1kHz

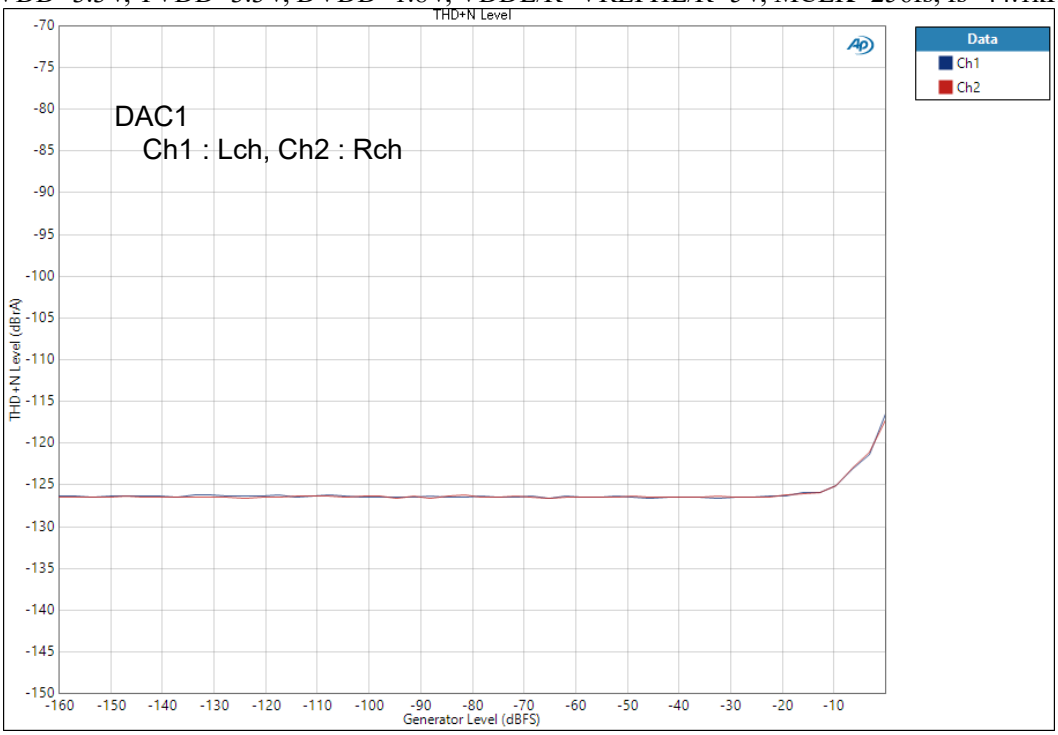


Plot Figure A-4. Out of Band Noise (“0” data Input)

fs = 44.1 kHz

AK4497S THD+N vs. Input Level

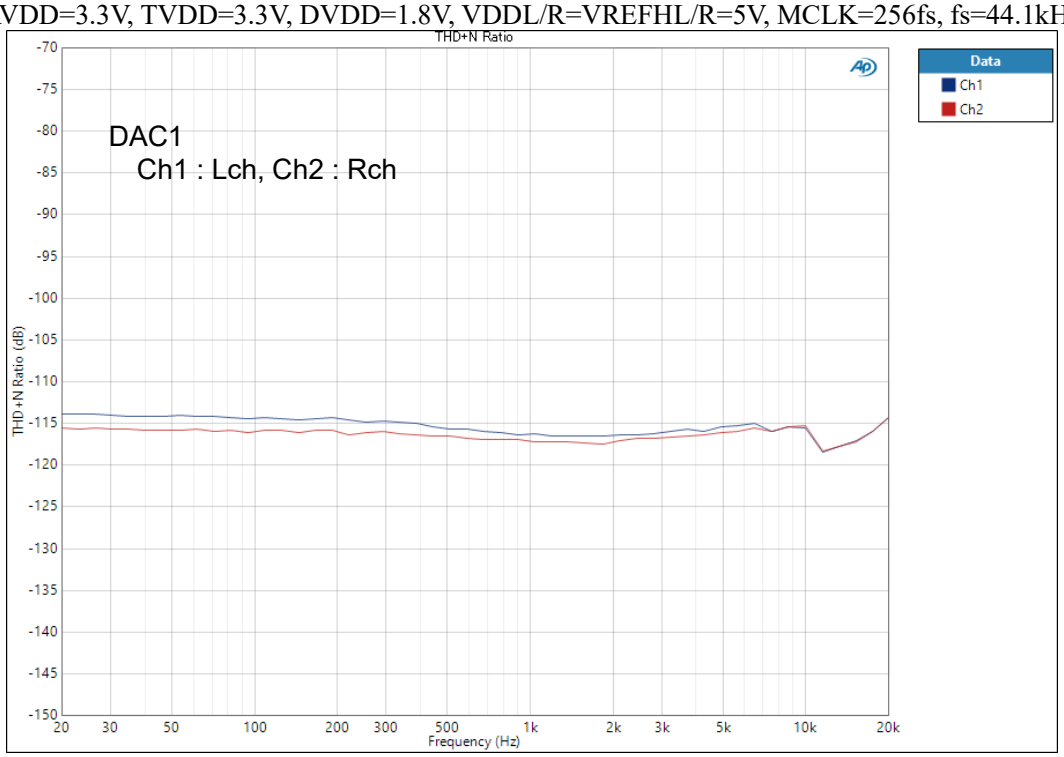
AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=44.1kHz



Plot Figure A-5. THD+N vs. Input Level

AK4497S THD+N vs. Input Frequency

AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=44.1kHz

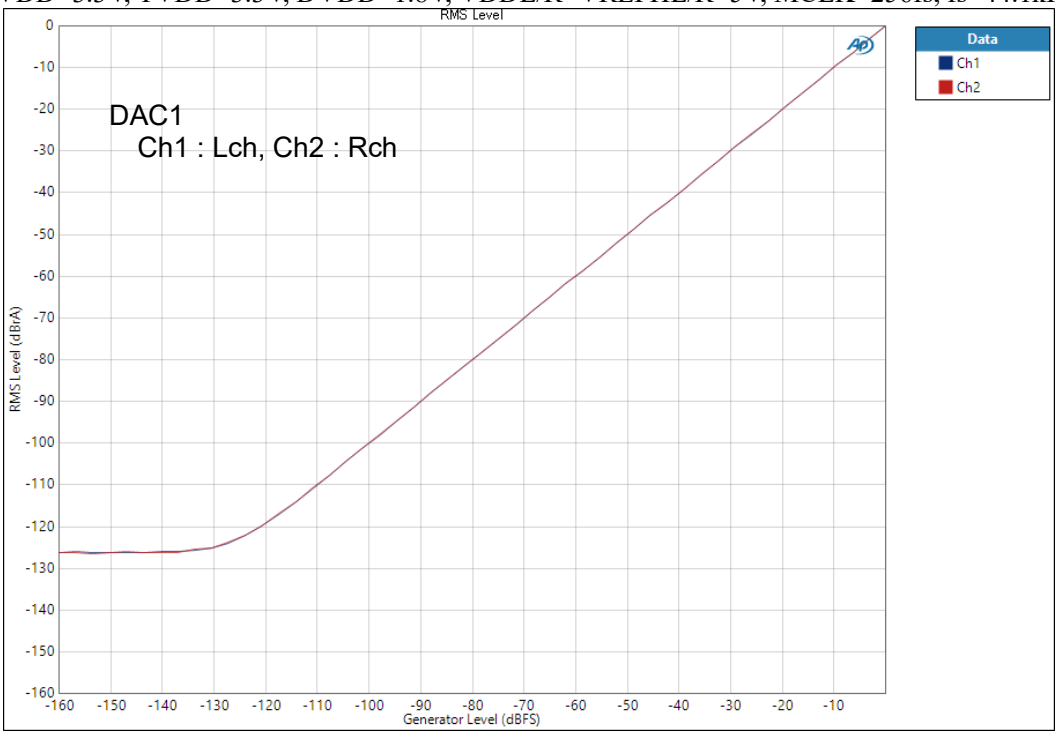


Plot Figure A-6. THD+N vs. Input Frequency

fs = 44.1 kHz

AK4497S Linearity

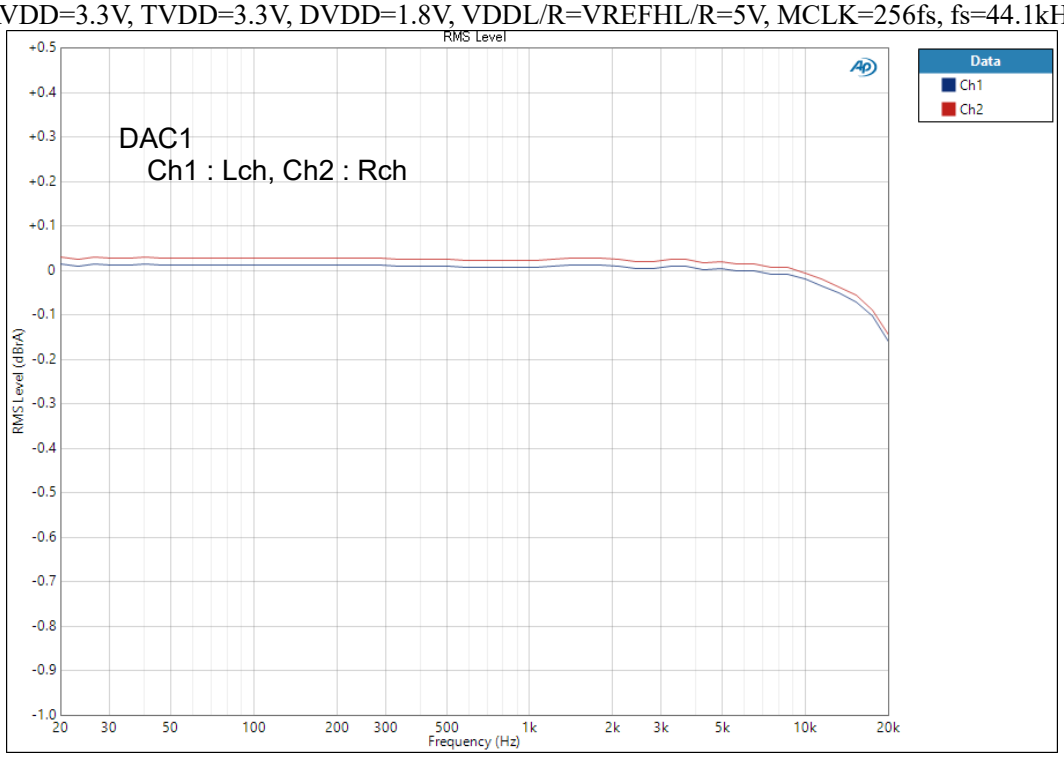
AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=44.1kHz



Plot Figure A-7. Linearity

AK4497S Frequency Response

AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=44.1kHz

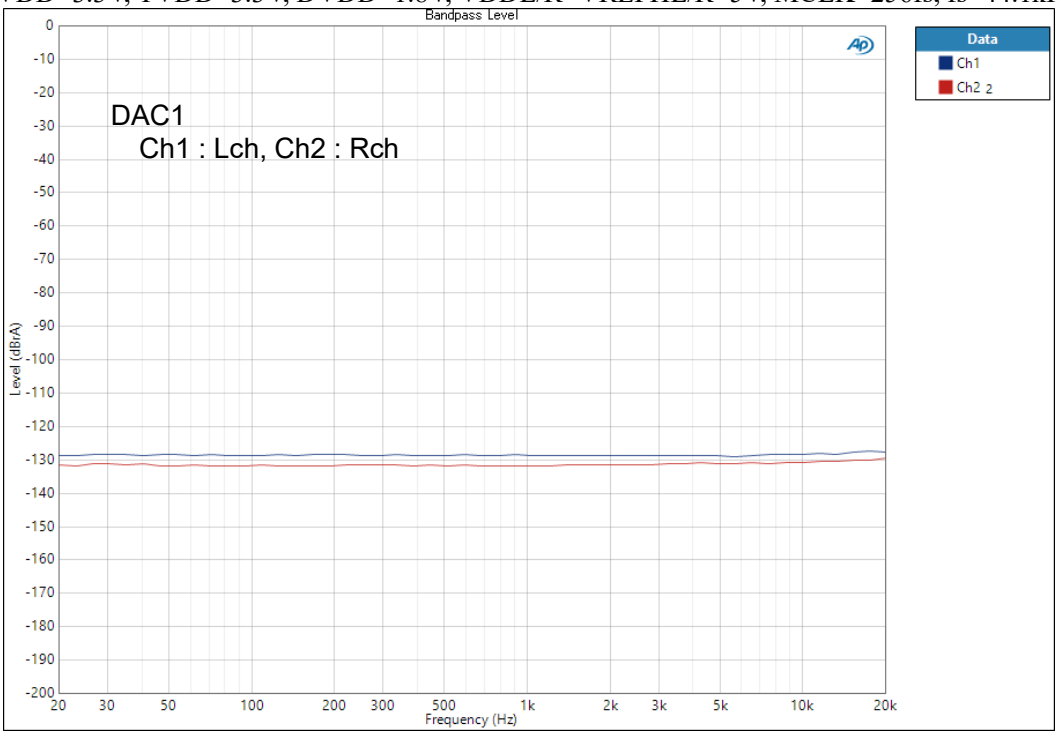


Plot Figure A-8. Frequency Response

fs = 44.1 kHz

AK4497S Crosstalk

AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=44.1kHz

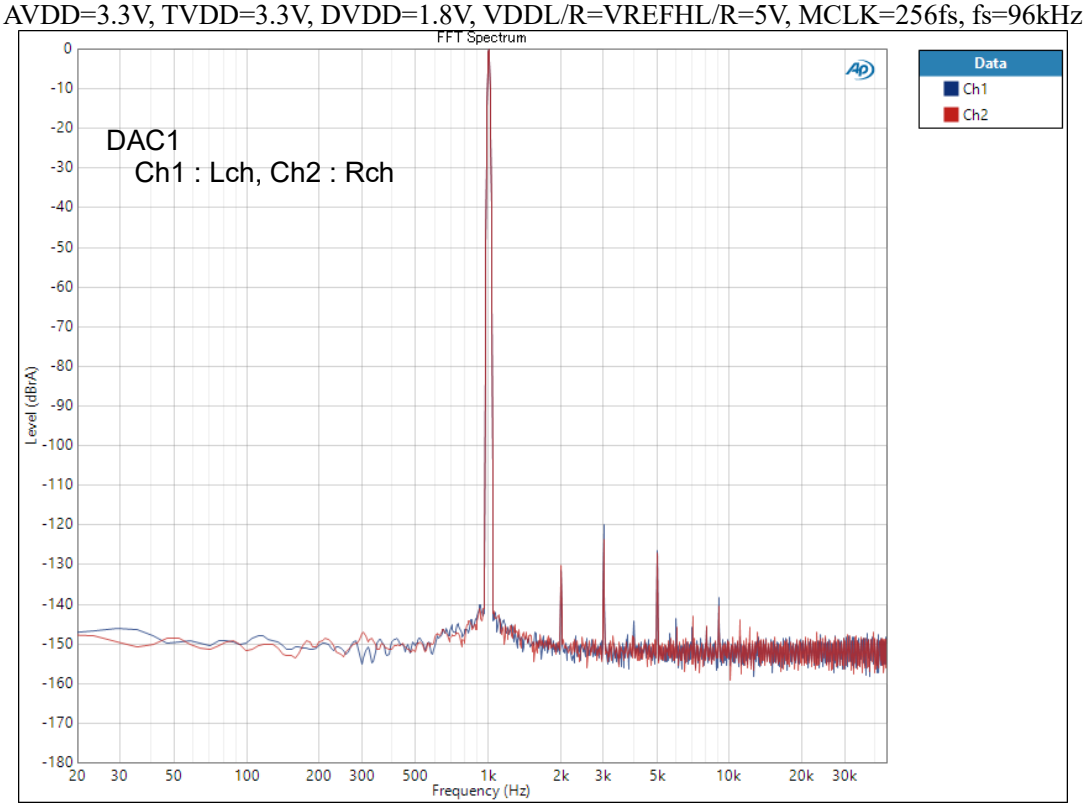


Plot Figure A-9. Crosstalk

fs = 96kHz

AK4497S FFT (0dBFS Input)

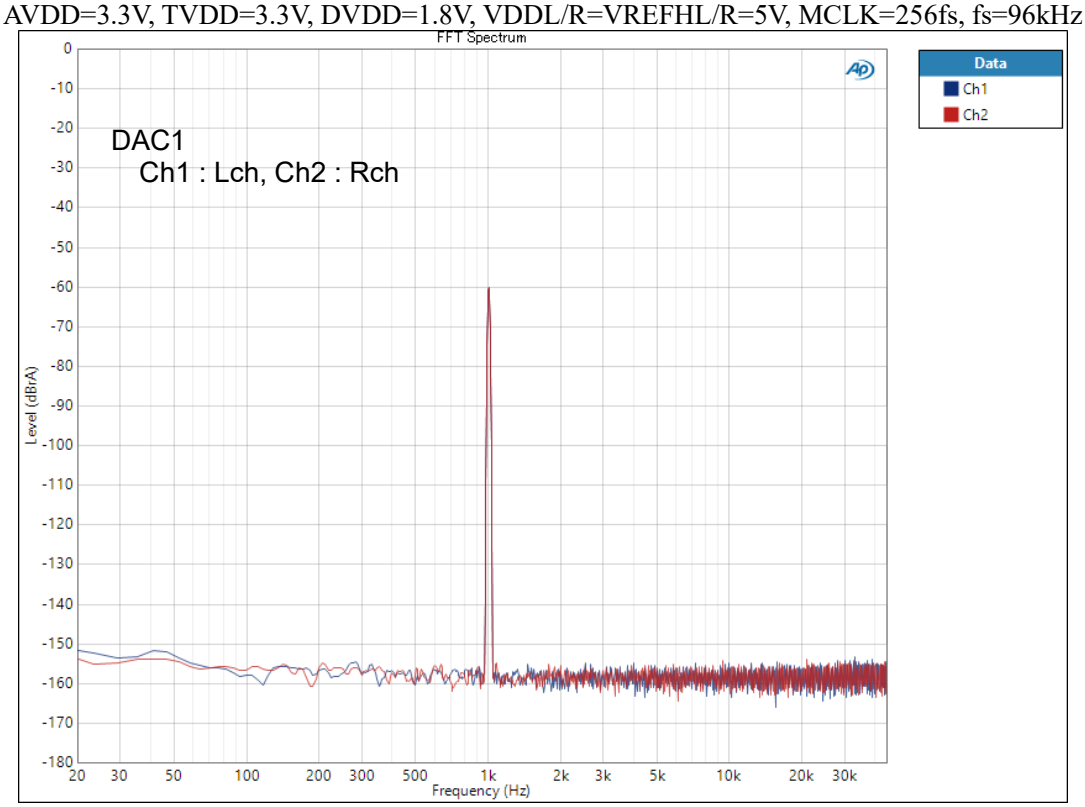
AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=96kHz



Plot Figure B-1. FFT (0dBFS Input)

AK4497S FFT (-60dBFS Input)

AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=96kHz

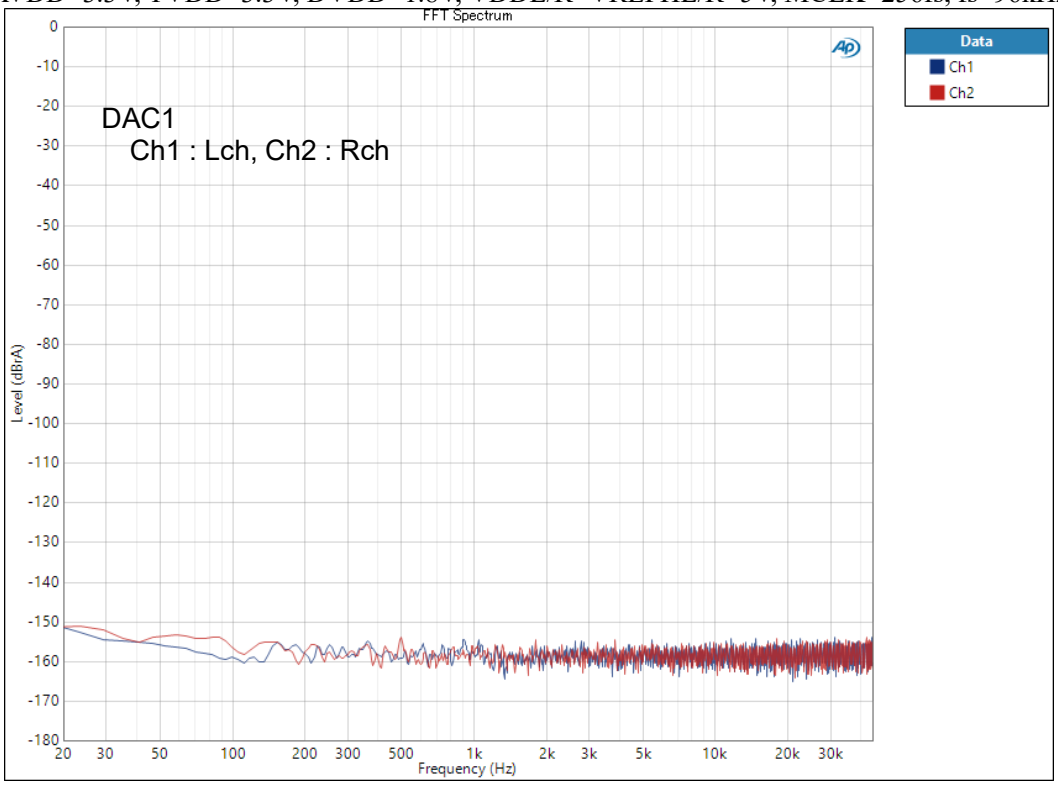


Plot Figure B-2. FFT (-60dBFS Input)

fs = 96kHz

AK4497S FFT (“0” data Input)

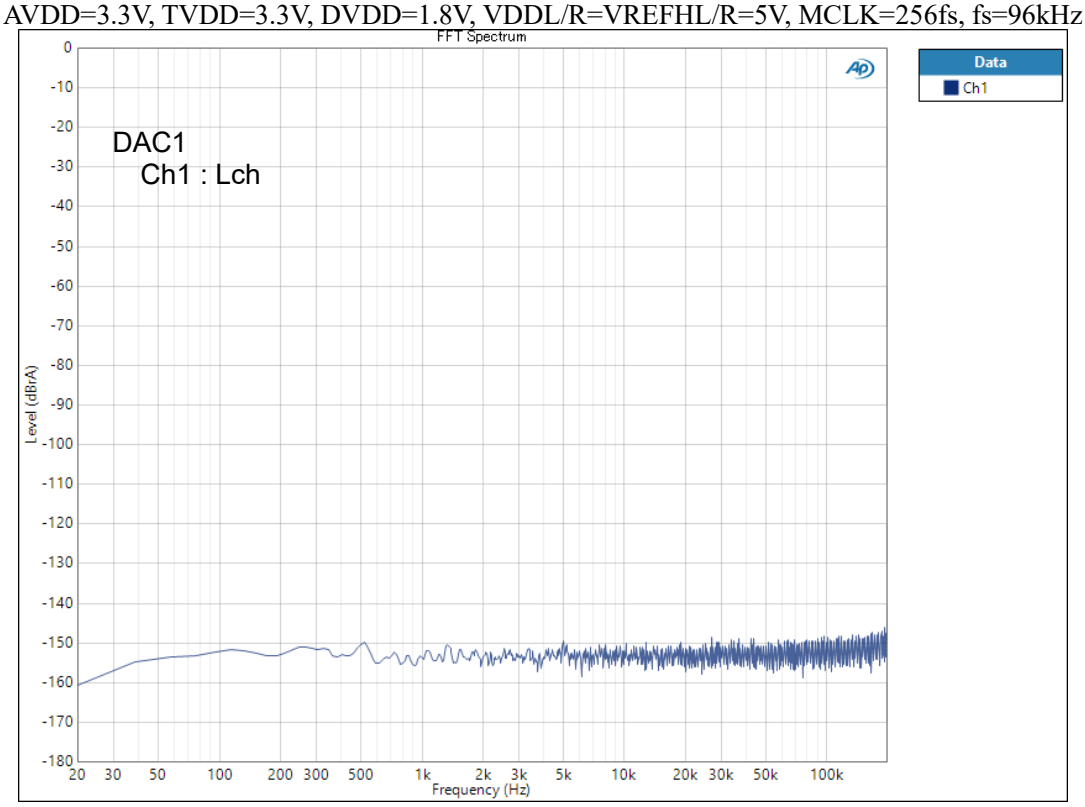
AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=96kHz



Plot Figure B-3. FFT (“0” data Input)

AK4497S Out of Band Noise (“0” data Input)

AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=96kHz

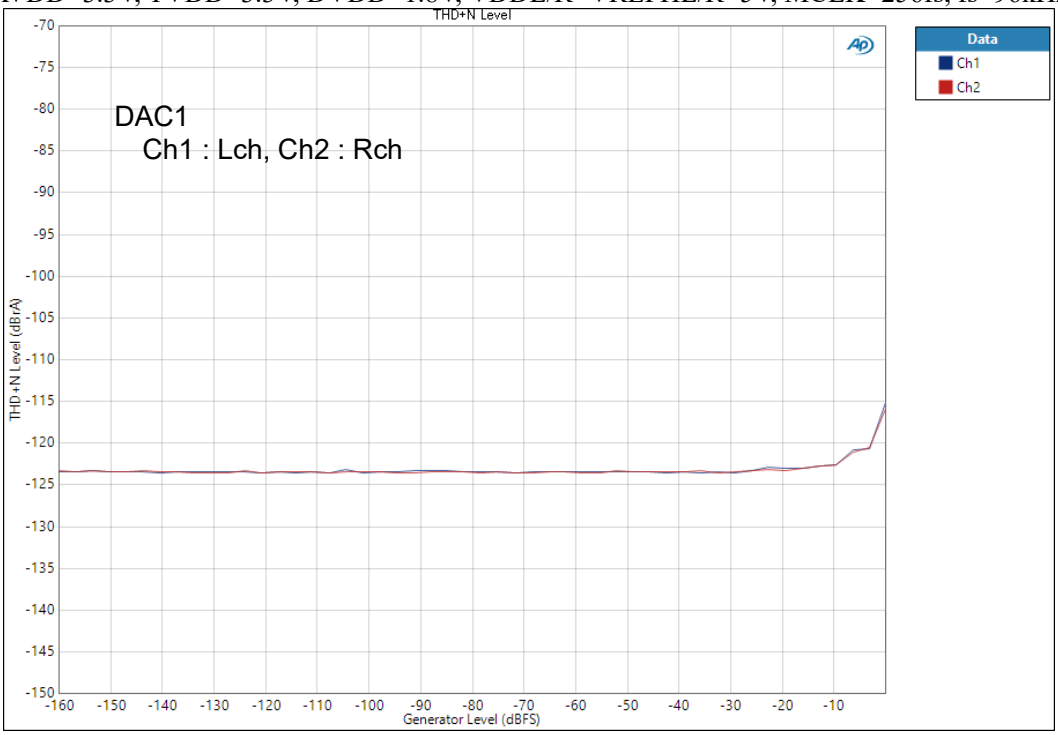


Plot Figure B-4. Out of Band Noise (“0” data Input)

fs = 96kHz

AK4497S THD+N vs. Input Level

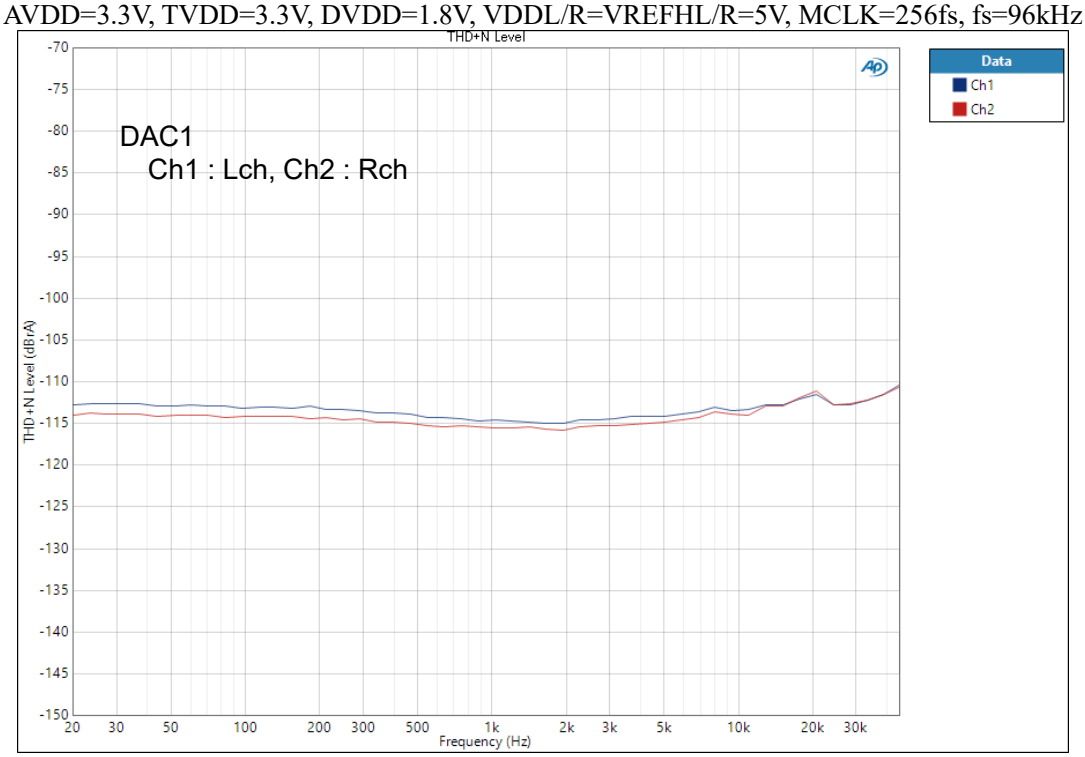
AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=96kHz



Plot Figure B-5. THD+N vs. Input Level

AK4497S THD+N vs. Input Frequency

AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=96kHz

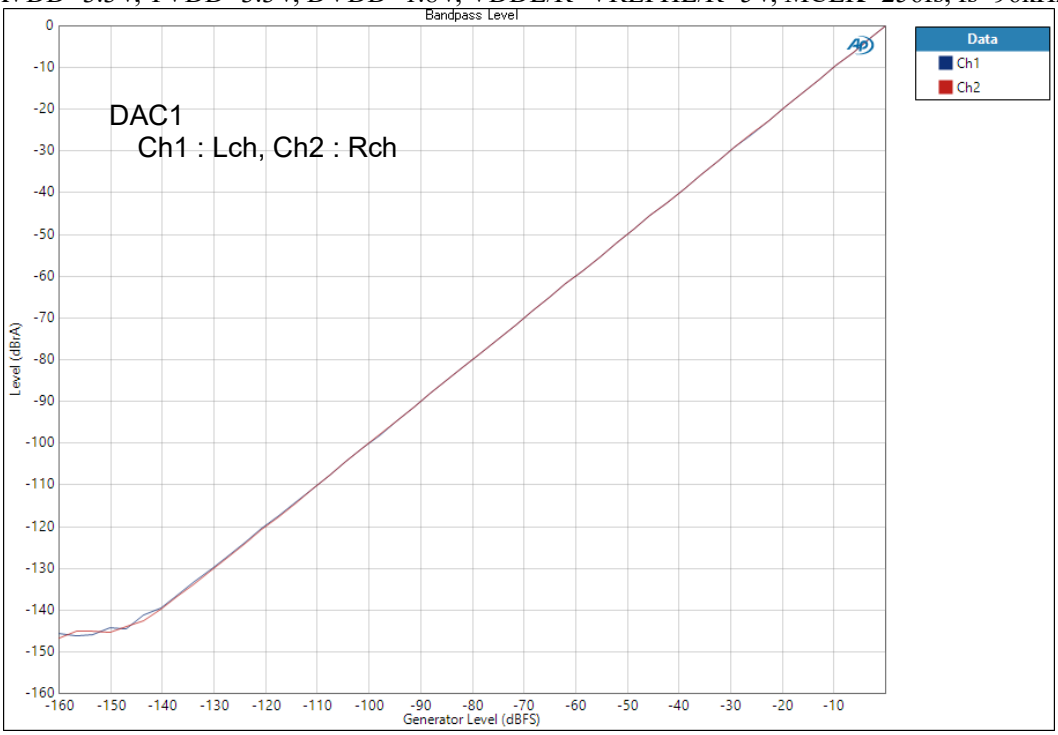


Plot Figure B-6. THD+N vs. Input Frequency

fs = 96kHz

AK4497S Linearity

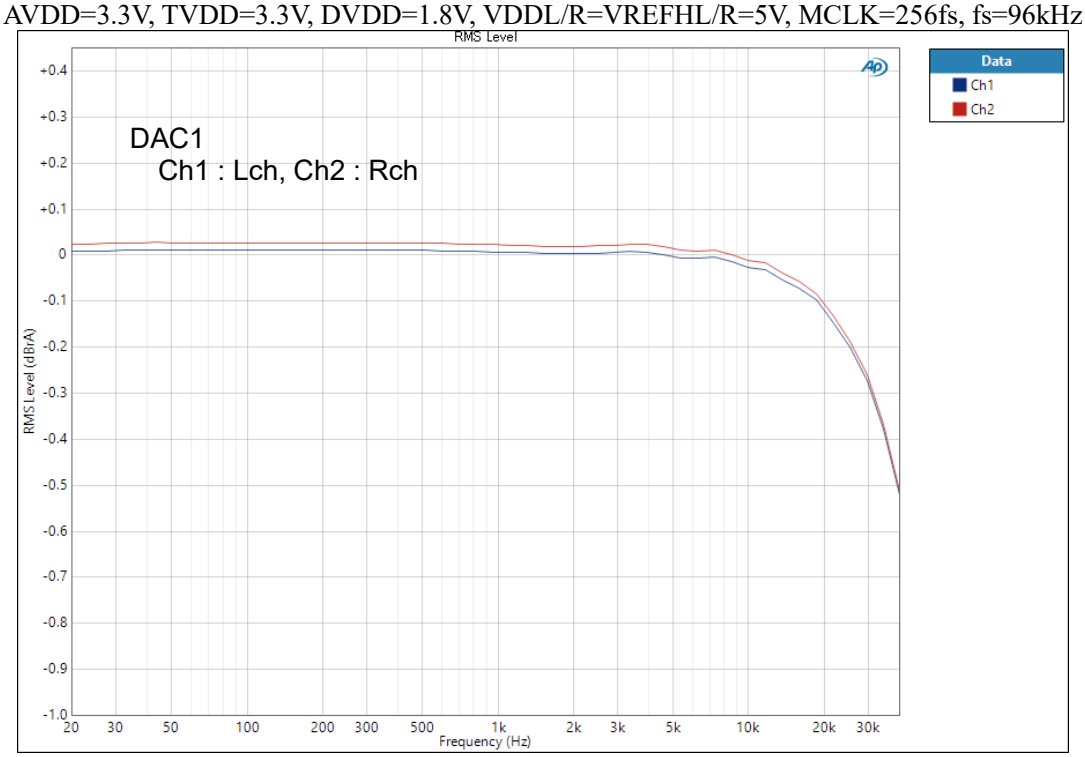
AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=96kHz



Plot Figure B-7. Linearity

AK4497S Frequency Response

AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=96kHz

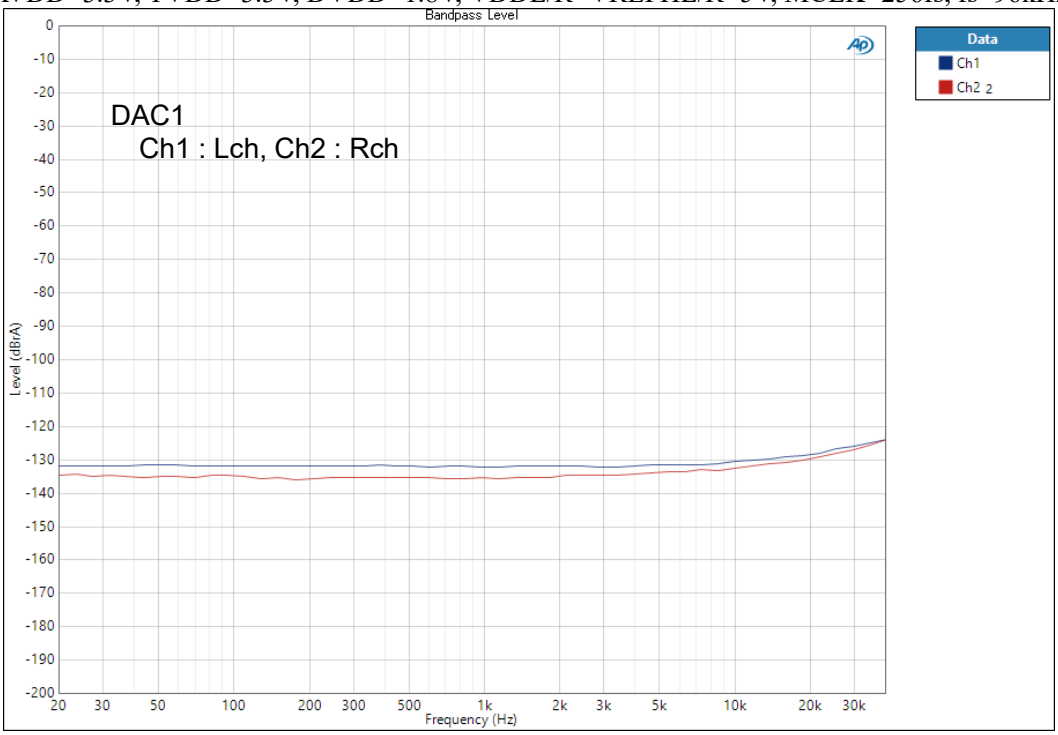


Plot Figure B-8. Frequency Response

fs = 96kHz

AK4497S Crosstalk

AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=256fs, fs=96kHz

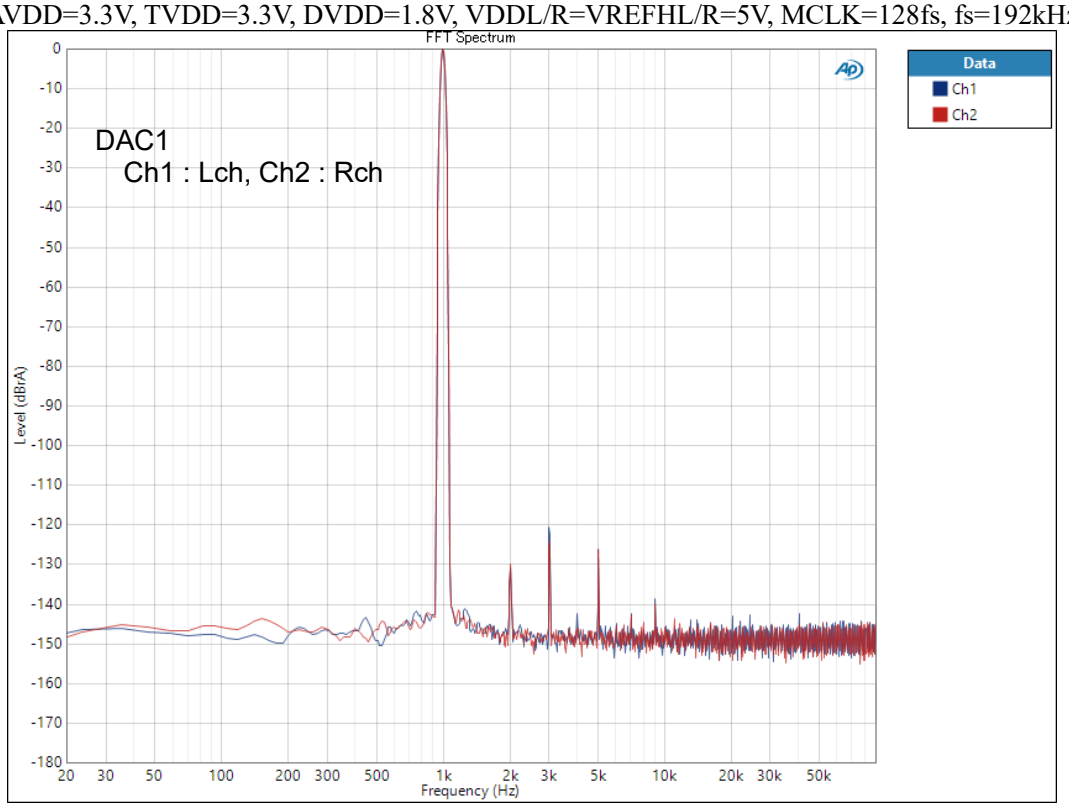


Plot Figure B-9. Crosstalk

fs = 192kHz

AK4497S FFT (0dBFS Input)

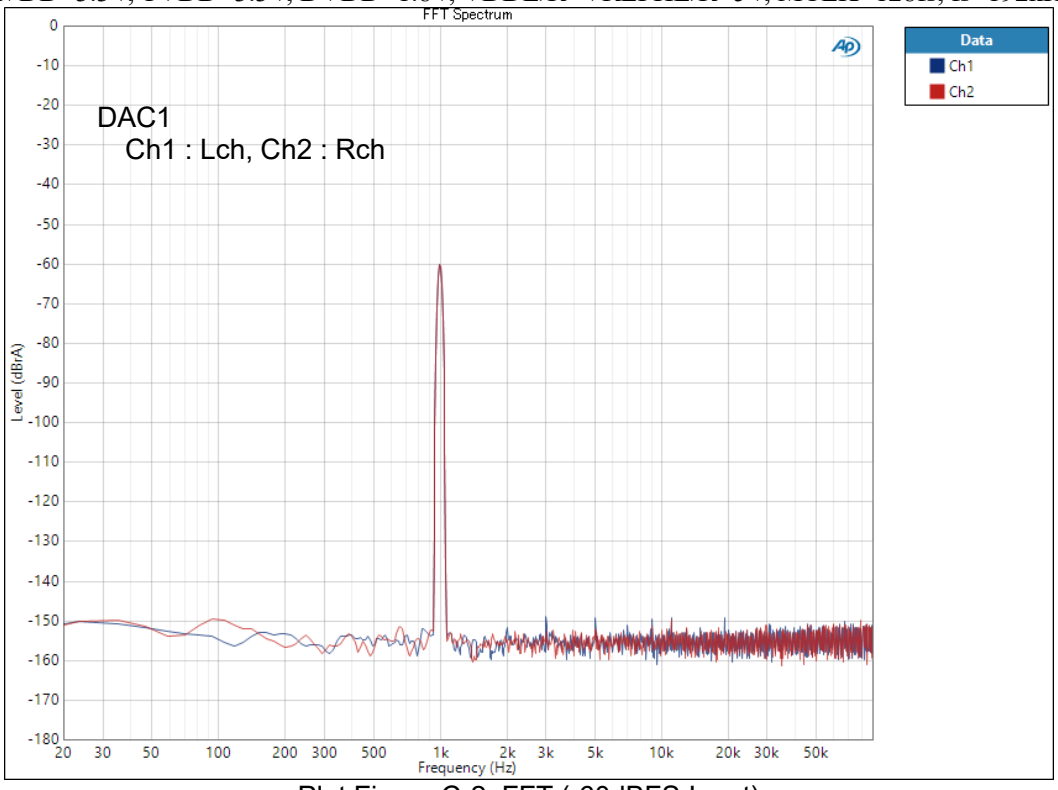
AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=192kHz



Plot Figure C-1. FFT (0dBFS Input)

AK4497S FFT (-60dBFS Input)

AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=192kHz

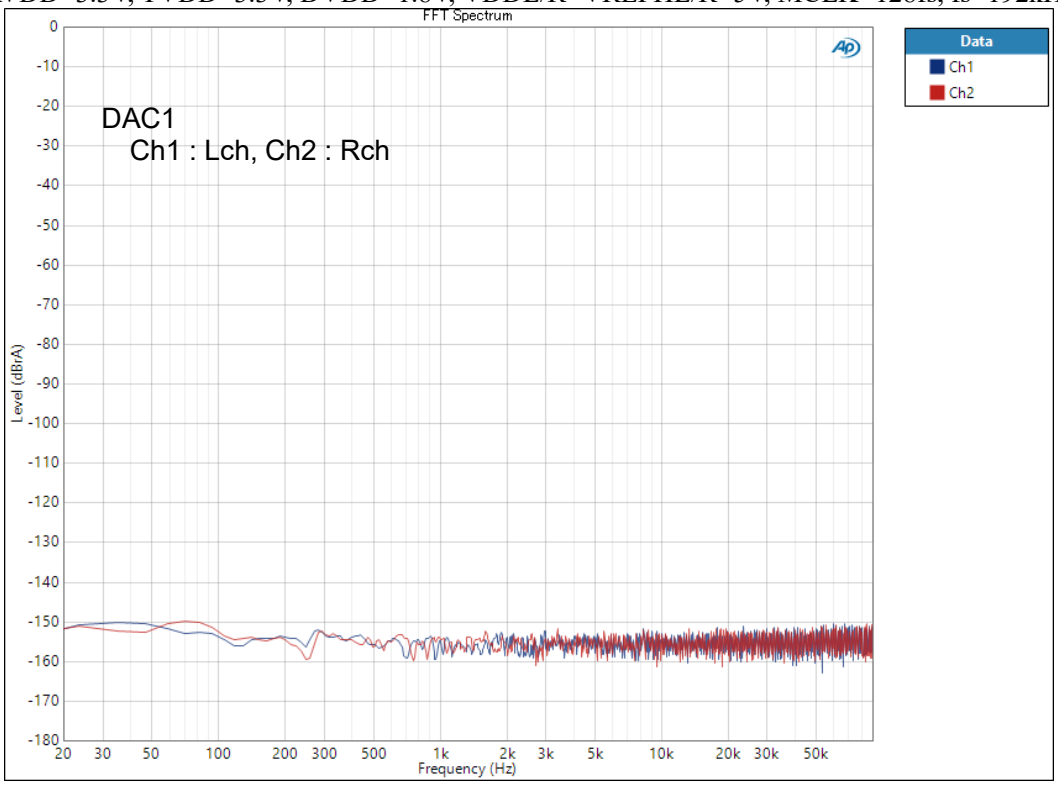


Plot Figure C-2. FFT (-60dBFS Input)

fs = 192kHz

AK4497S FFT (“0” data Input)

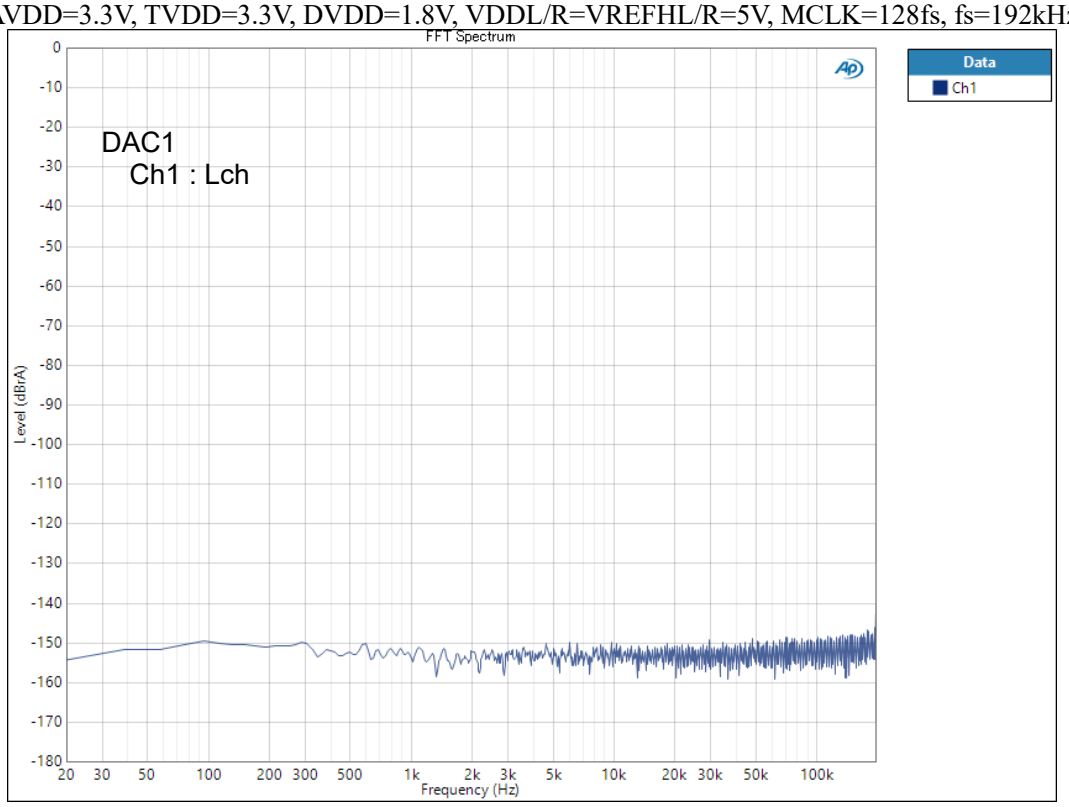
AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=192kHz



Plot Figure C-3. FFT (“0” data Input)

AK4497S Out of Band Noise (“0” data Input)

AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=192kHz

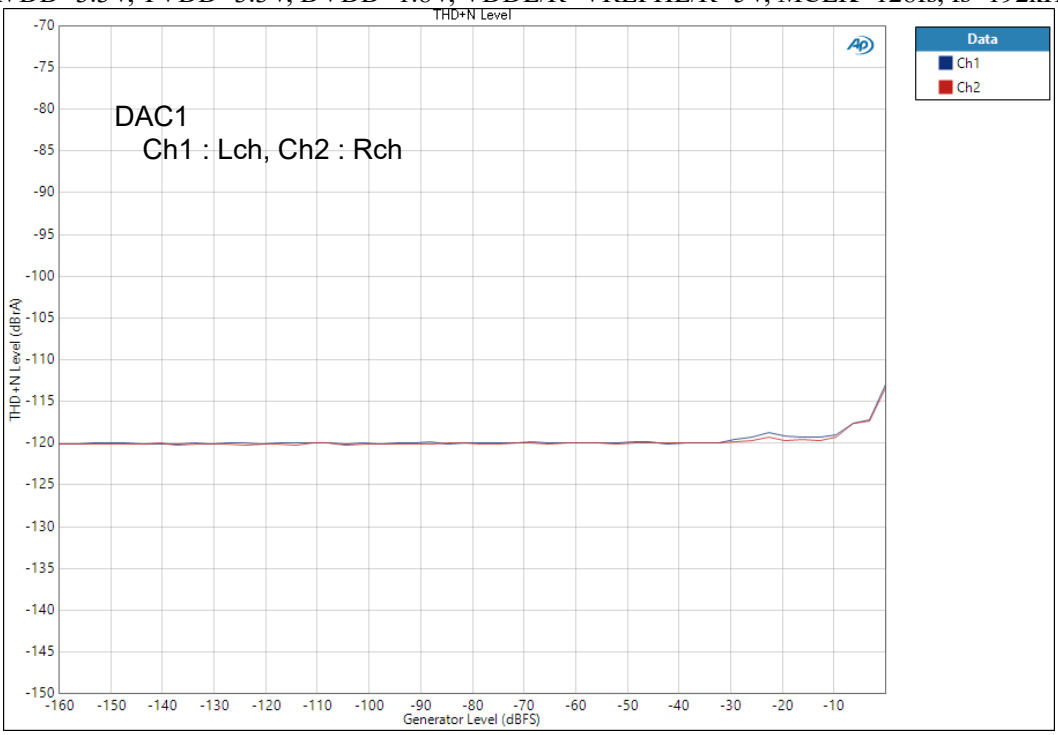


Plot Figure C-4. Out of Band Noise (“0” data Input)

fs = 192kHz

AK4497S THD+N vs. Input Level

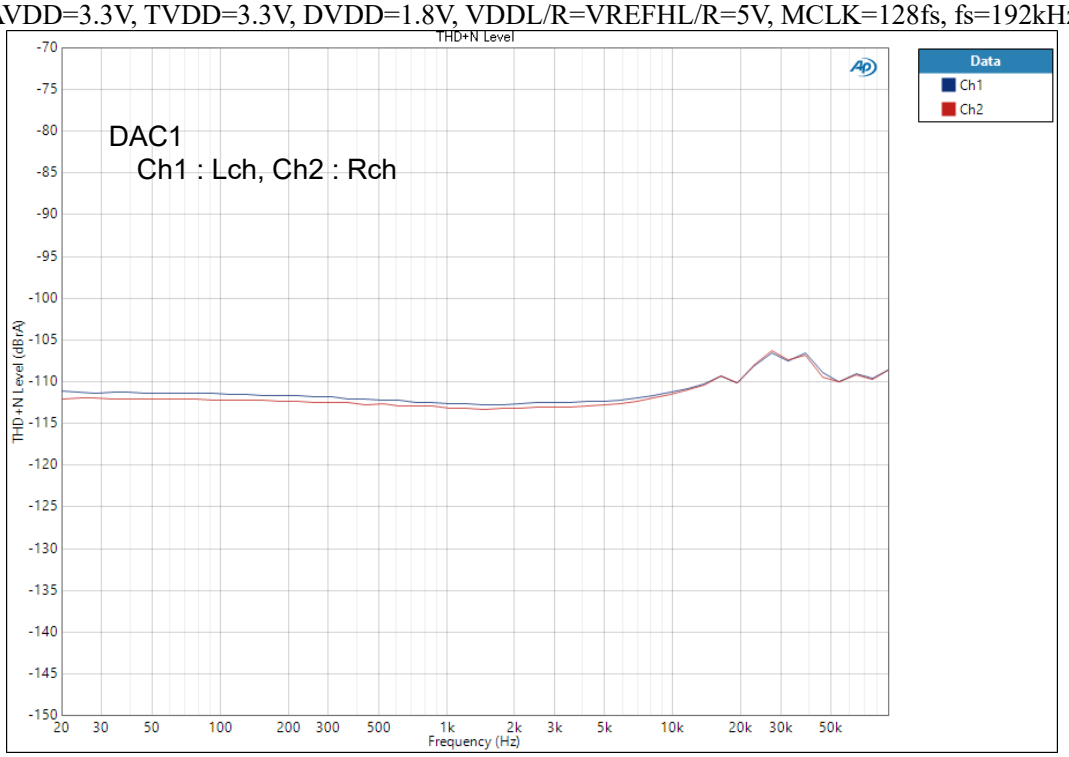
AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=192kHz



Plot Figure C-5. THD+N vs. Input Level

AK4497S THD+N vs. Input Frequency

AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=192kHz

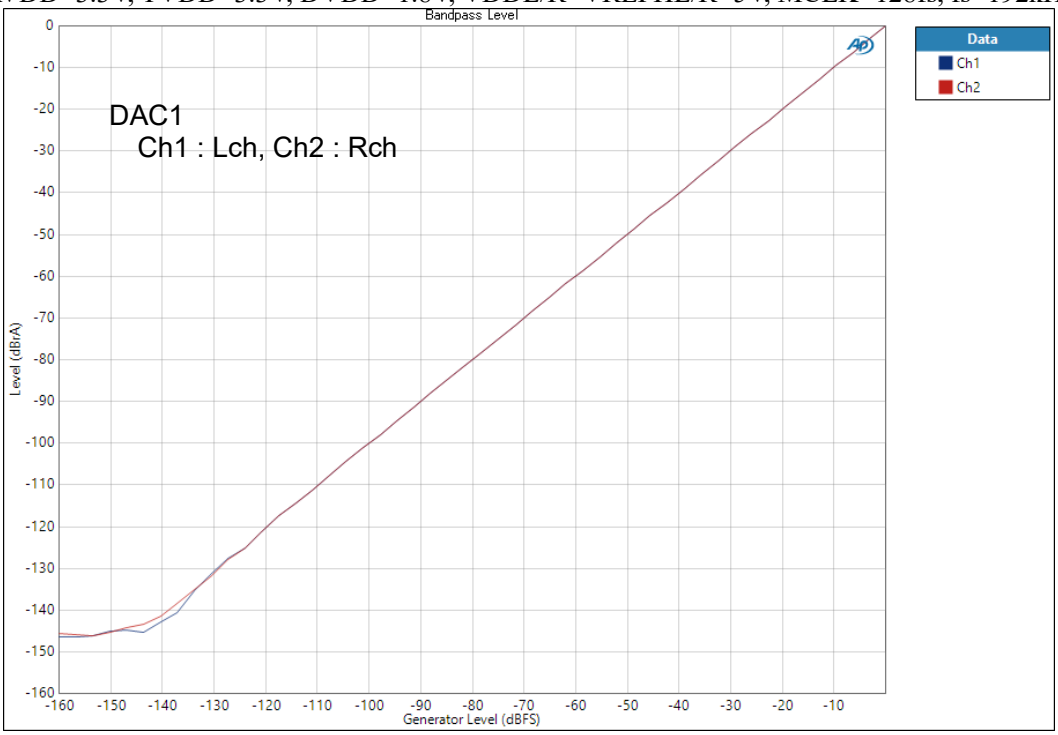


Plot Figure C-6. THD+N vs. Input Frequency

fs = 192kHz

AK4497S Linearity

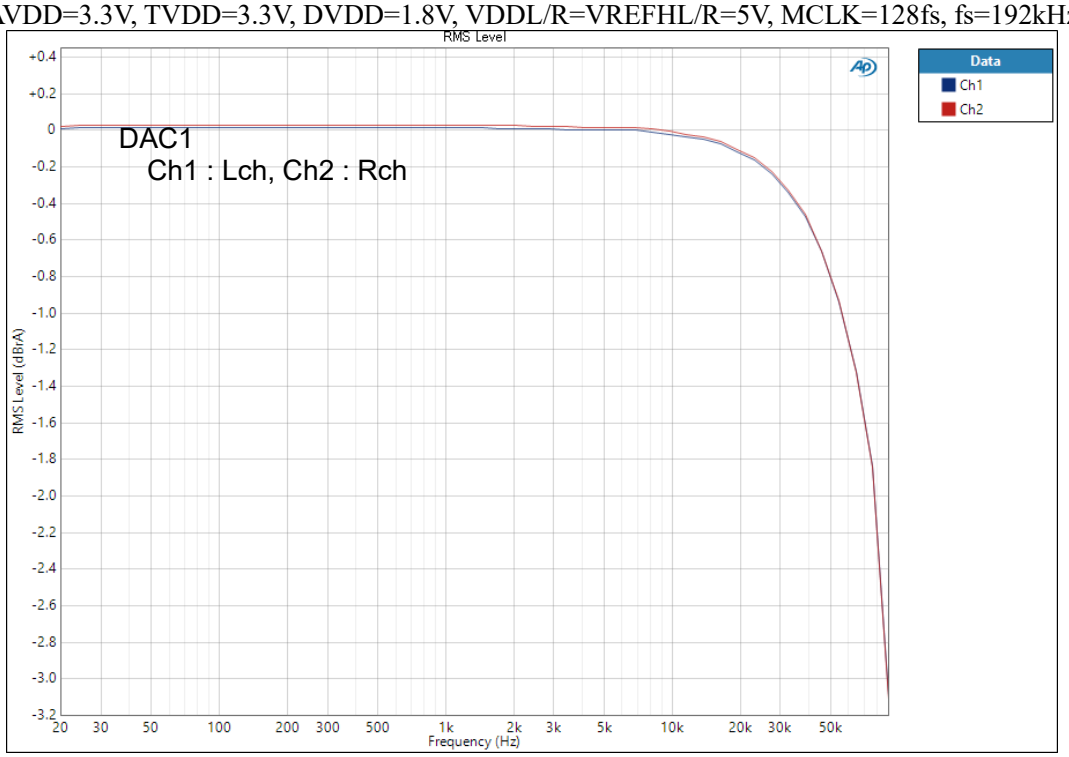
AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=192kHz



Plot Figure C-7. Linearity

AK4497S Frequency Response

AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=192kHz

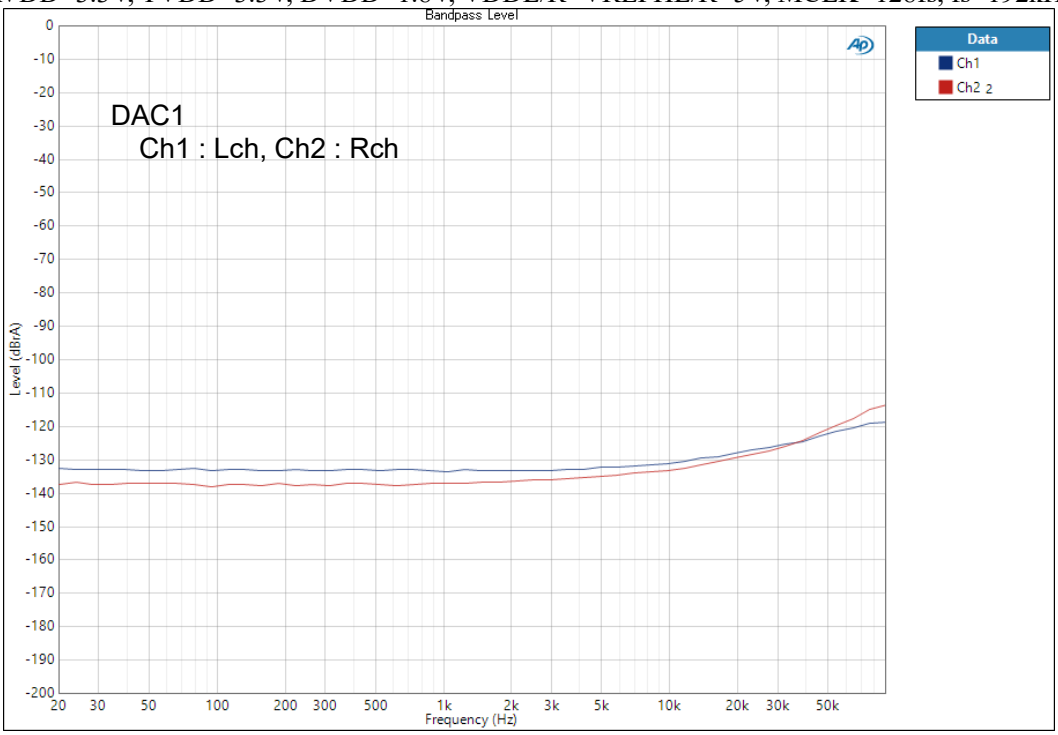


Plot Figure C-8. Frequency Response

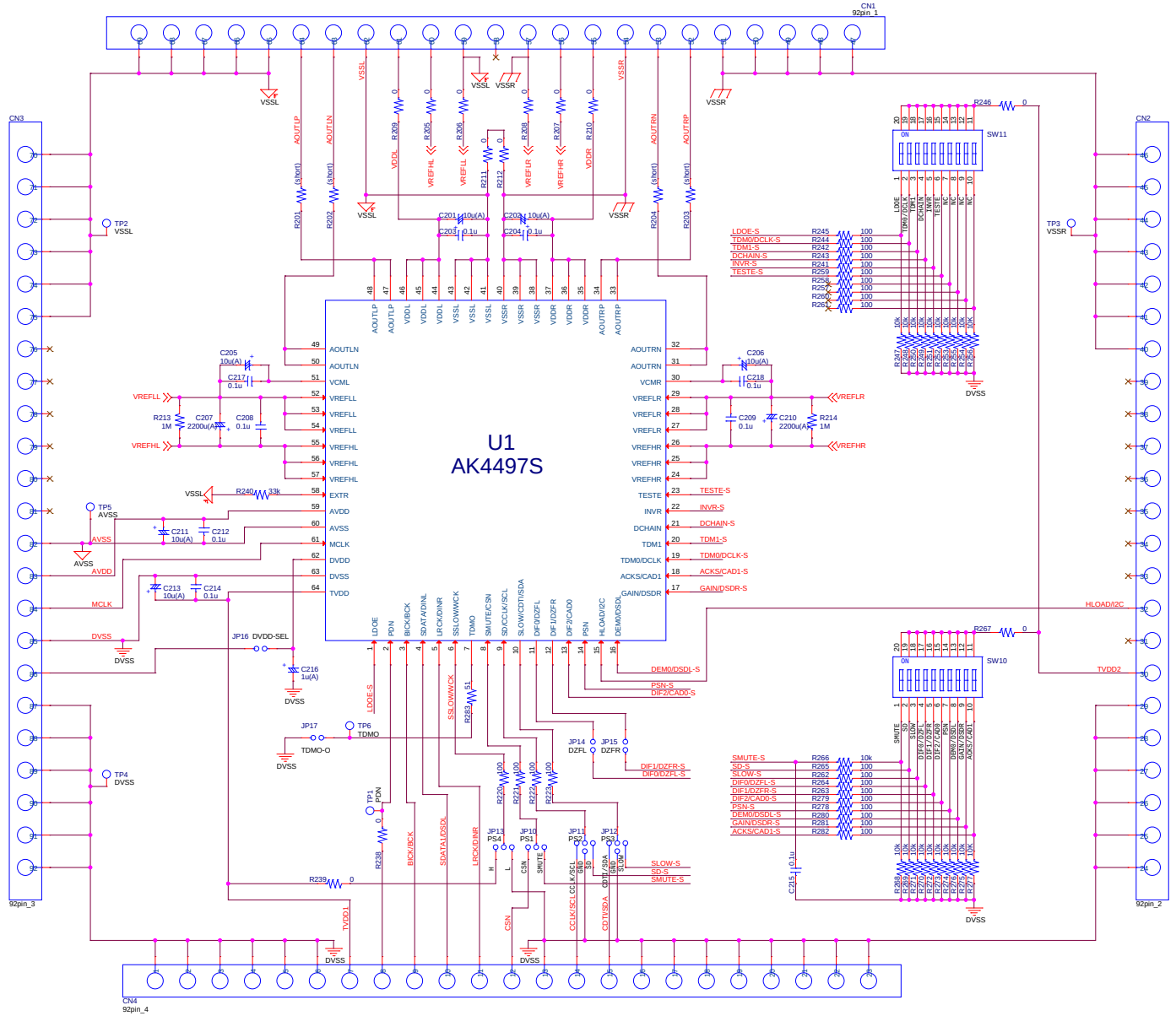
fs = 192kHz

AK4497S Crosstalk

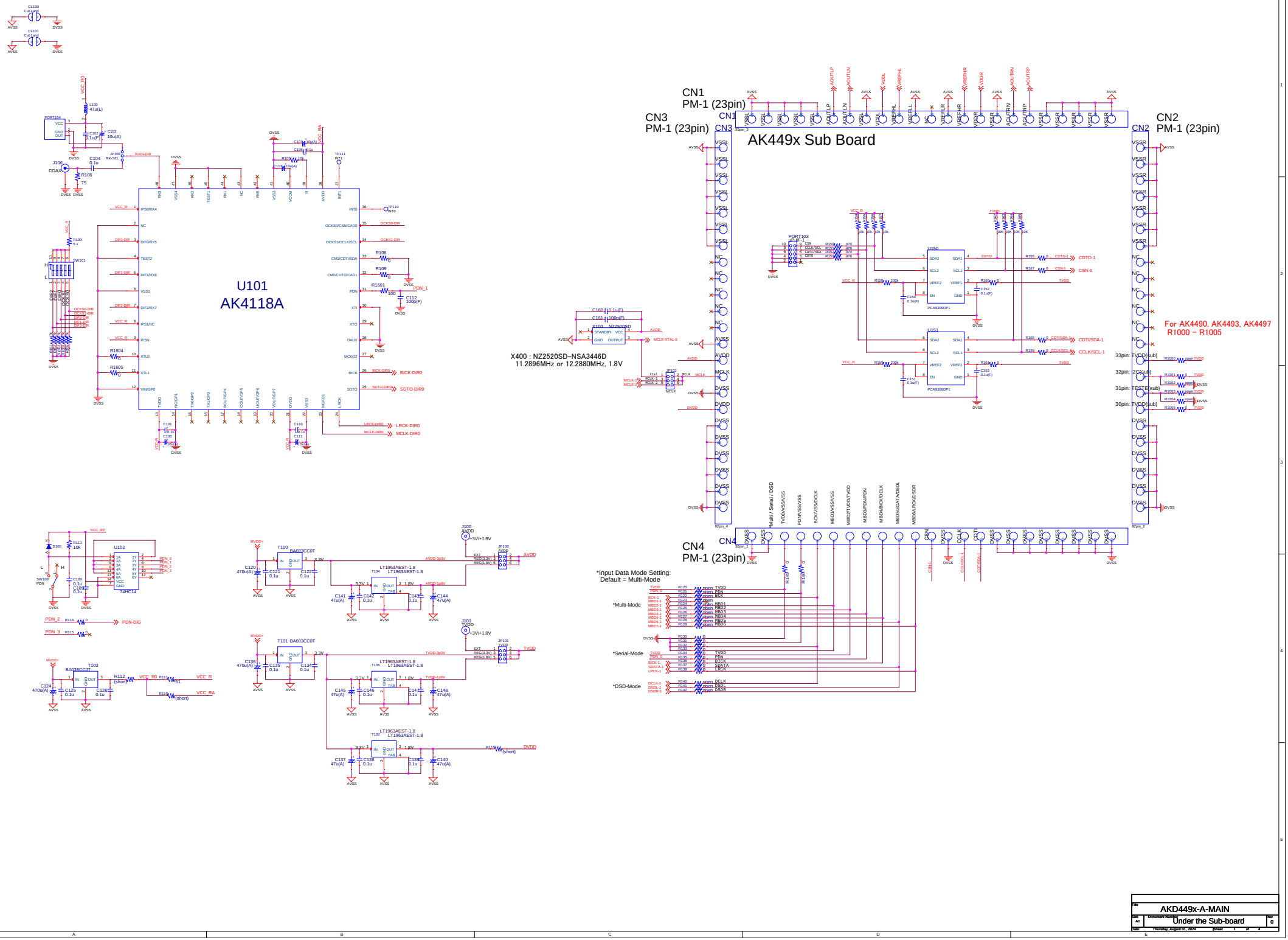
AVDD=3.3V, TVDD=3.3V, DVDD=1.8V, VDDL/R=VREFHL/R=5V, MCLK=128fs, fs=192kHz



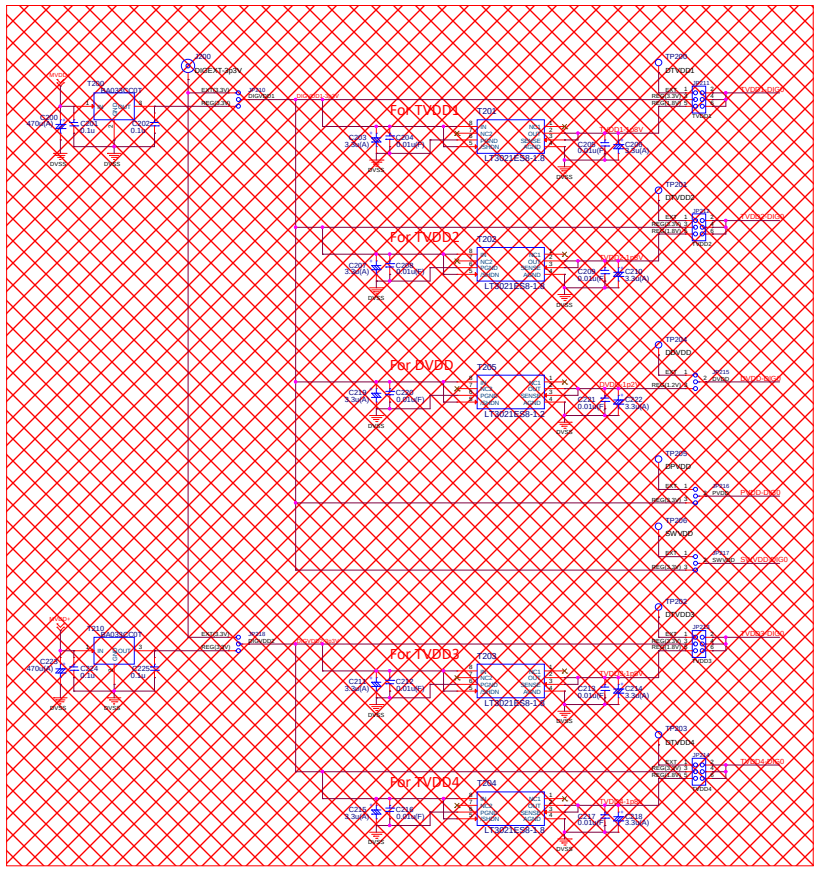
Plot Figure C-9. Crosstalk



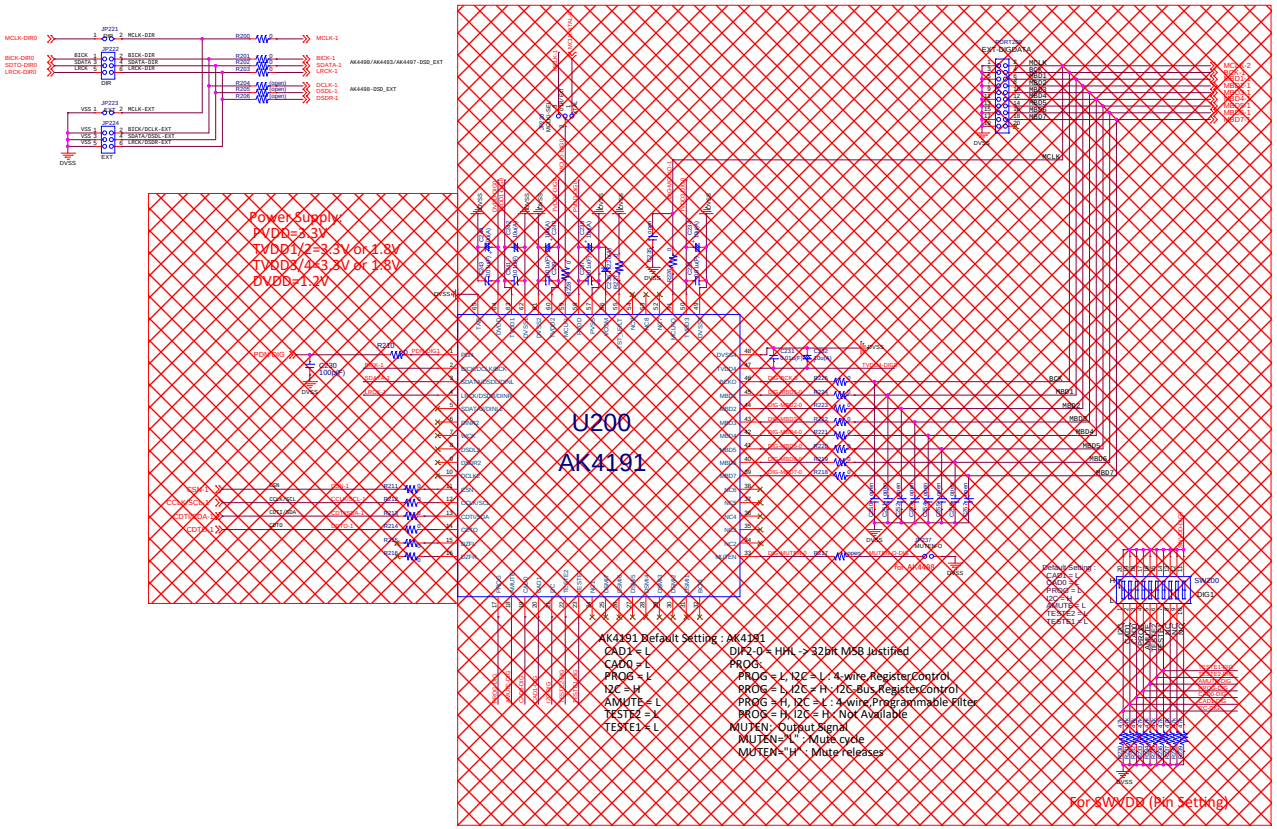
Title	AKD4497-A-SUB		
Size A2	Document Number AK4497		Rev 2
Date: Wednesday, October 30, 2024	Sheet 1 of 1		


U101
AK4118A
AK449x Sub Board
CN1
PM-1 (23pin)
CN2
PM-1 (23pin)
CN3
PM-1 (23pin)
CN4
PM-1 (23pin)
For AK4490, AK4493, AK4497
R1000 − R1005
X400 : NZ2520SD−NSA3446D
11.2896MHz or 12.2880MHz, 1.8V
U102
74HC14
U150
PCA9306DP1
U151
PCA9306DP1
*Input Data Mode Setting:
Default = Multi-Mode
*Multi-Mode
*Serial-Mode
*DSD-Mode
AKD449x-A-MAIN
Under the Sub-board

AK4191 Digital-IC Block

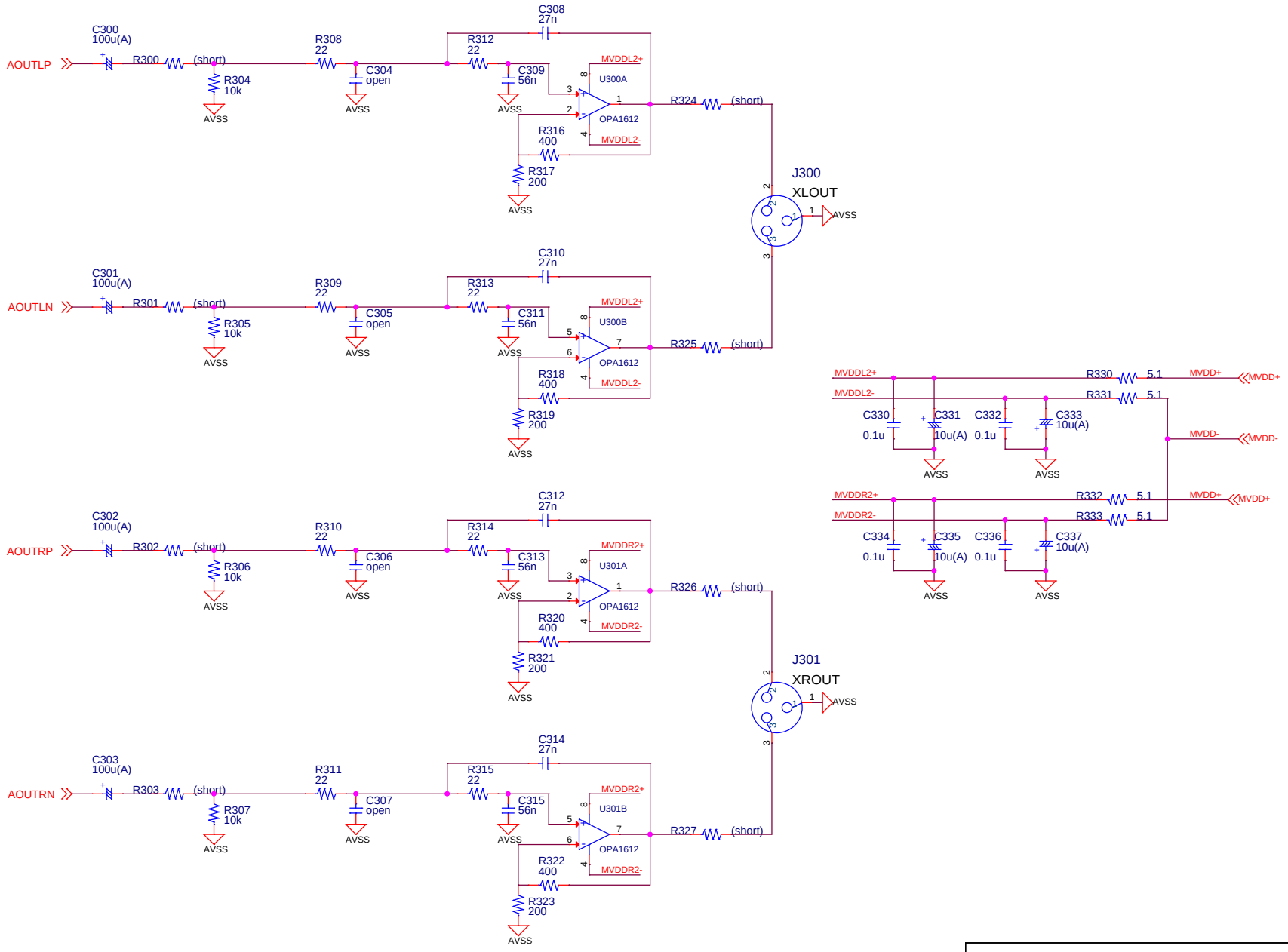


Parts no mounted

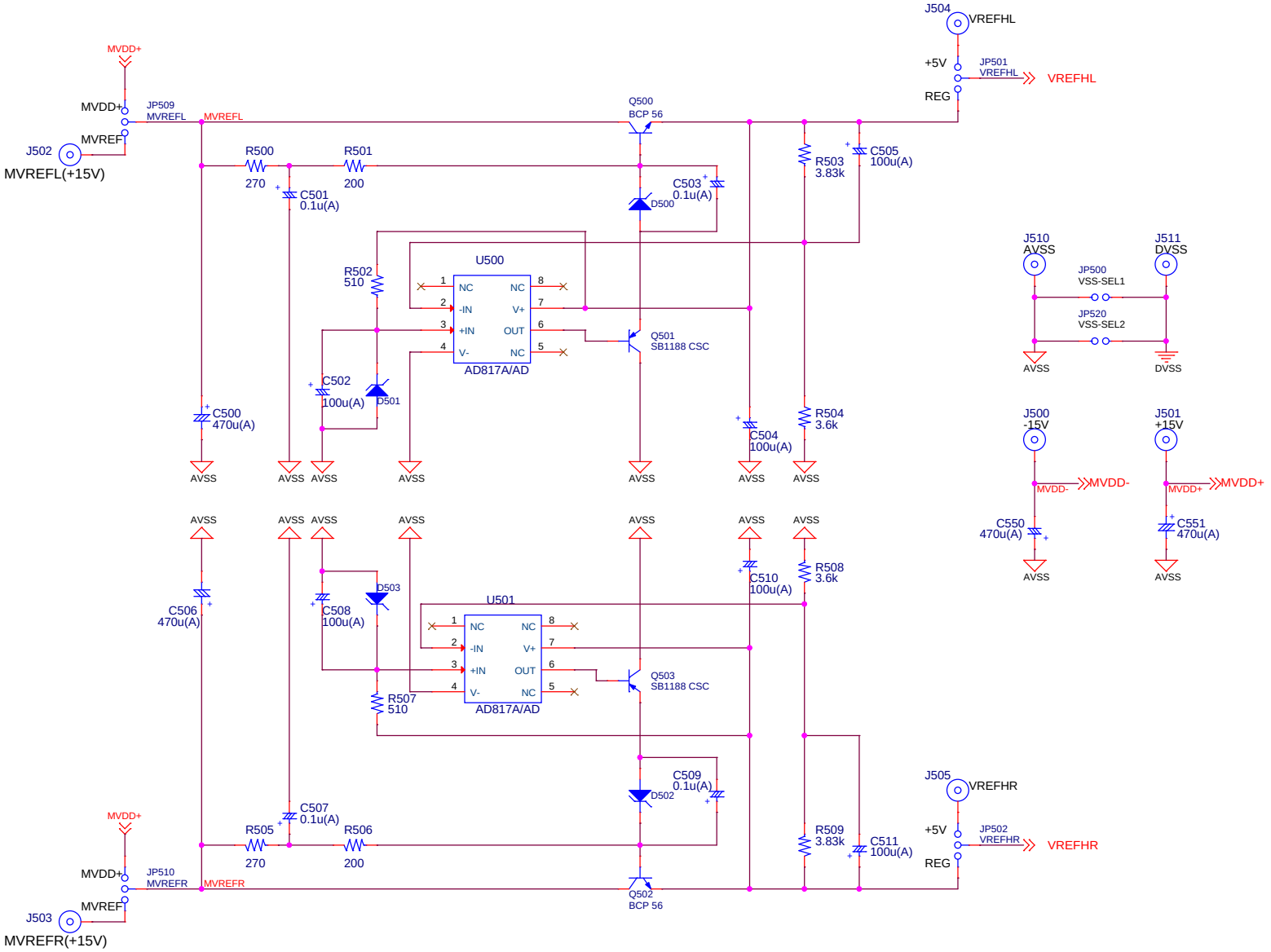


Parts no mounted

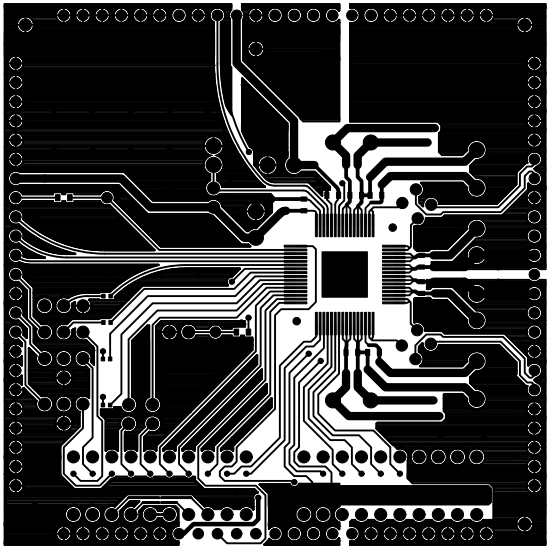
Title	AKD449x-A-MAIN		
Size A1	Document Number AK4191		Rev 0
Date: Thursday, August 01, 2024	Sheet 2 of 4		

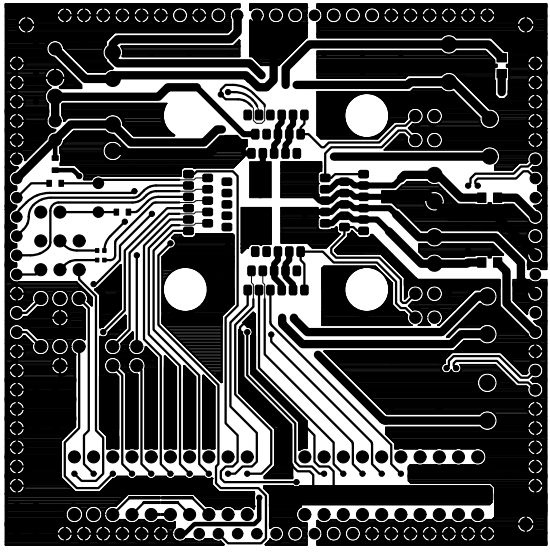


Title	AKD449x-A-MAIN	
Size A3	Document Number: External LPF2 Analog Output	Rev 0
Date: Thursday, August 01, 2024	Sheet 3 of 4	

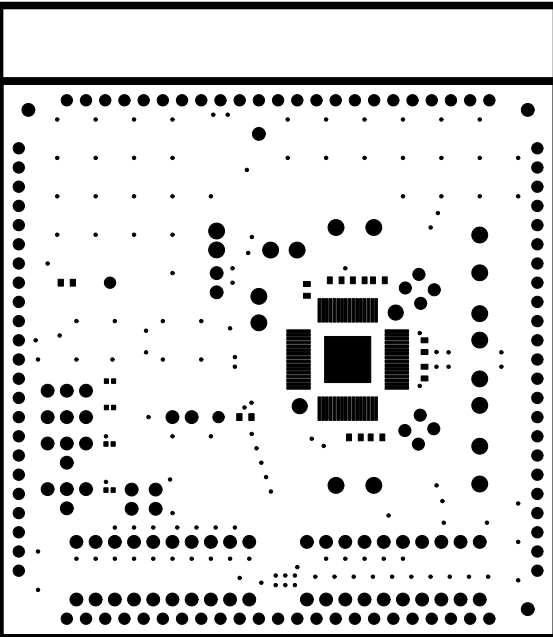


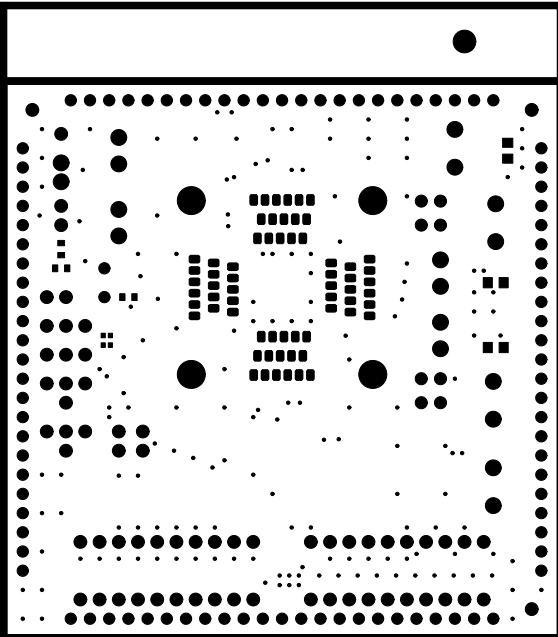
Title	AKD449x-A-MAIN	
Size A3	Document Number Power Supply Unit	Rev 0
Date: Thursday, August 01, 2024	Sheet 4 of 4	



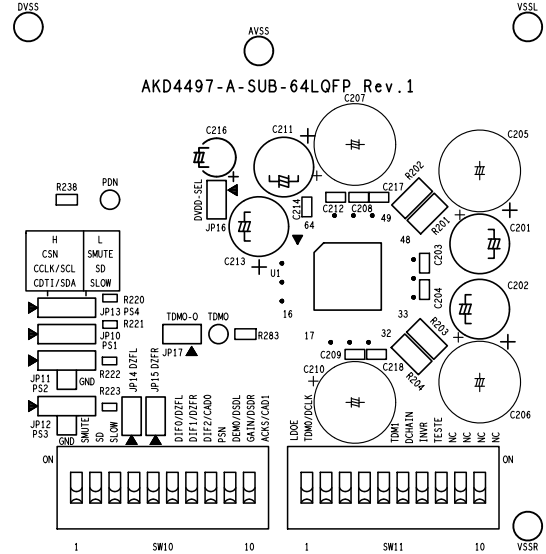


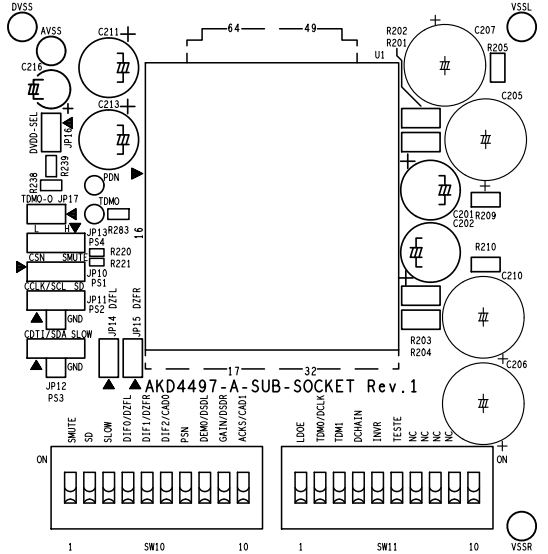
AKD4497-A-SUB PATTERN-S LZ 3312015IA-01



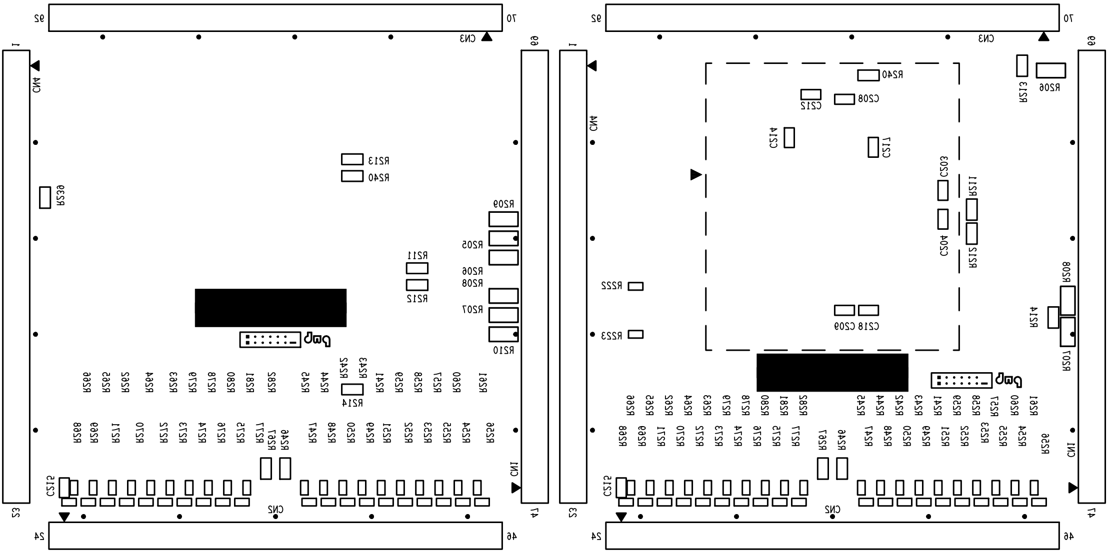


AKD4497-A-SUB SOLDER-RESIST-S 331201S1A-01


DVSS
AVSS
VSSL
AKD4497-A-SUB-64LQFP Rev.1
C207
C216
C211
C205
DVDD-SEL
JP16
C214
C212
C208
C217
R202
R201
C201
C213
U1
C203
C204
C202
R238
PDN
H
CSN
CCLK/SCL
CDTI/SDA
L
SMUTE
SD
SLOW
R220
JP13 PS4
R221
JP10 PS1
JP11 PS2
GND
R222
JP14 DZFL
JP15 DZFR
JP12 PS3
R223
TDMO-O
TDMO
JP17
R283
R203
R204
C209
C218
C210
C206
64
49
48
33
32
17
16
SMUTE
SD
SLOW
DIF0/DZFL
DIF1/DZFR
DIF2/CAD0
PSN
DEM0/DSDL
GAIN/DSDR
ACKS/CAD1
LDOE
TDMO/DCLK
TDMI
DCHAIN
INVR
TESTE
NC
ON
1
SW10
10
SW11
VSSR

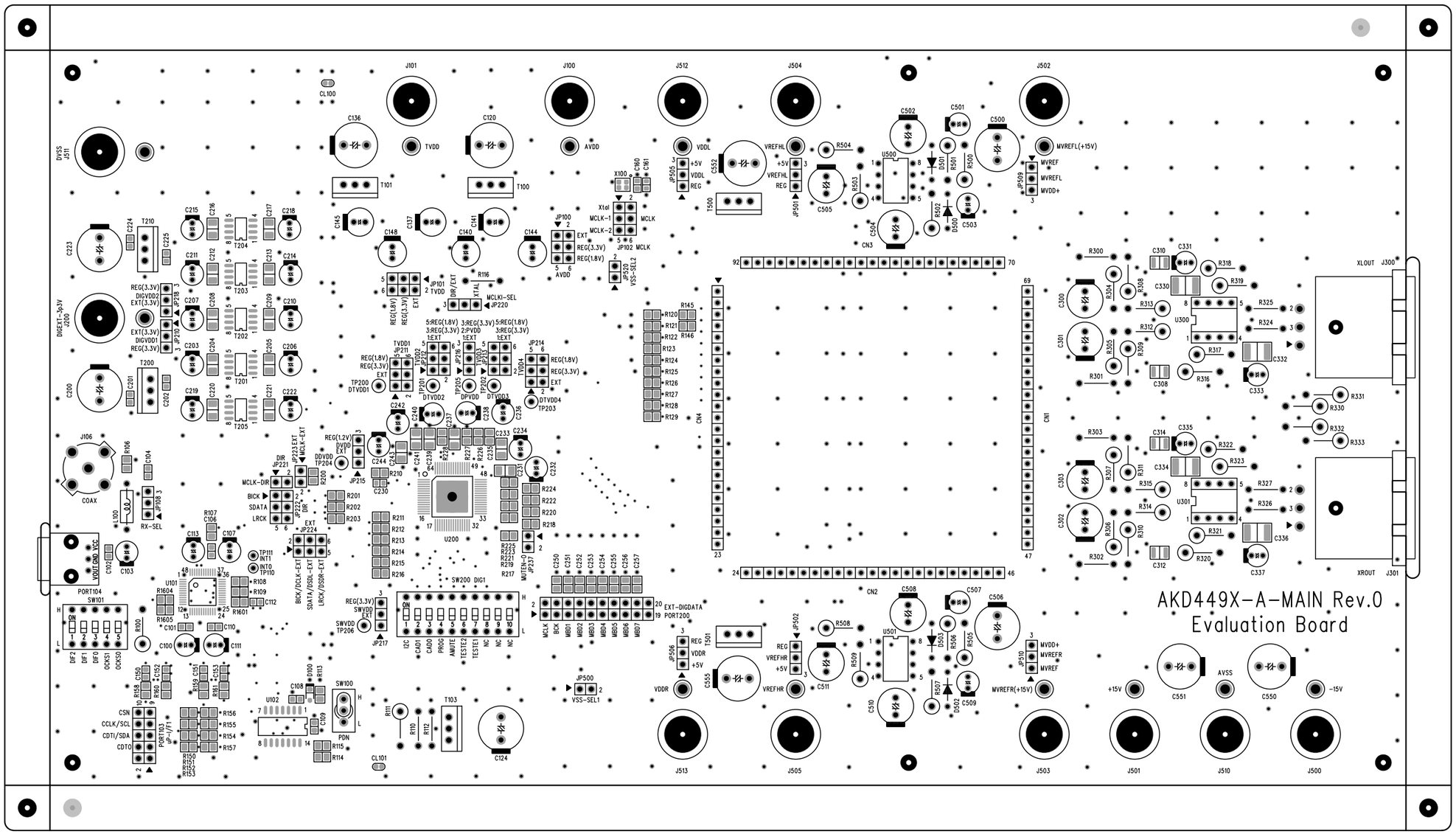

DVSS
AVSS
VSSL
64
49
C211
C216
C213
R202
R201
U1
C207
R205
C205
DVDD-SEL
JP16
R239
PDN
R238
TDMO-O
JP17
TDMO
R283
C201
R209
C202
JP13 PS4
R220
CSN
SMUTE
JP10 PS1
R221
R210
CCLK/SCL
SDA
JP11 PS2
GND
JP14 DZFL
JP15 DZFR
C210
CDTI/SDA
SLOW
R203
R204
JP12 PS3
C206
17
32
AKD4497-A-SUB-SOCKET Rev.1
SMUTE
SD
SLOW
DIF0/DZFL
DIF1/DZFR
DIF2/CAD0
PSN
DEM0/DSDL
GAIN/DSDR
ACKS/CAD1
LDOE
TDMO/DCLK
TDMI
DCHAIN
INVR
TESTE
NC
ON
1
SW10
10
SW11
VSSR

AKD4497-A-SUB SYMBOL-PRINT-S 33120151A-01



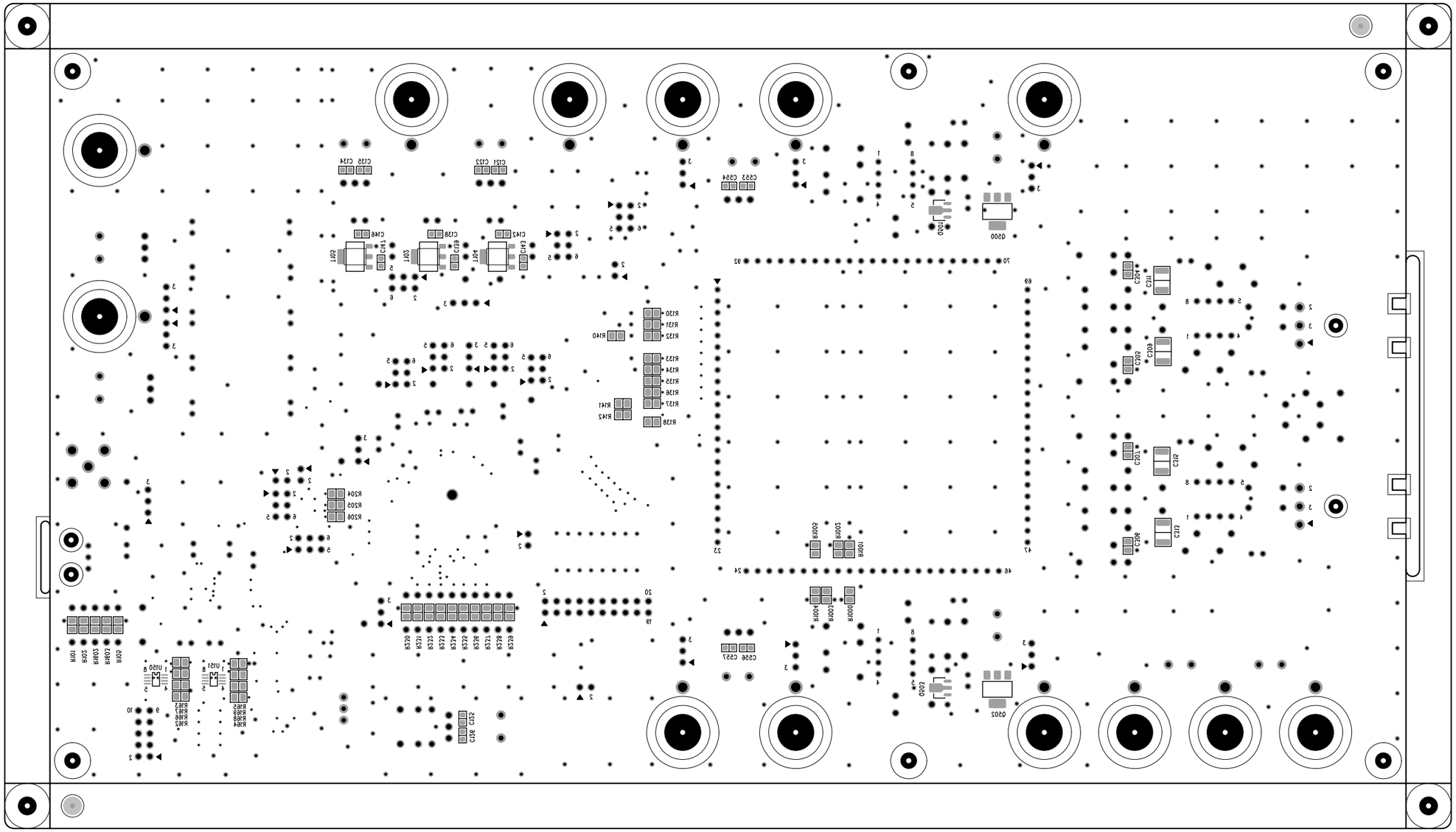
AKD449X-A-MAIN_Rev.0

部品面シルク図　　部品面透視図



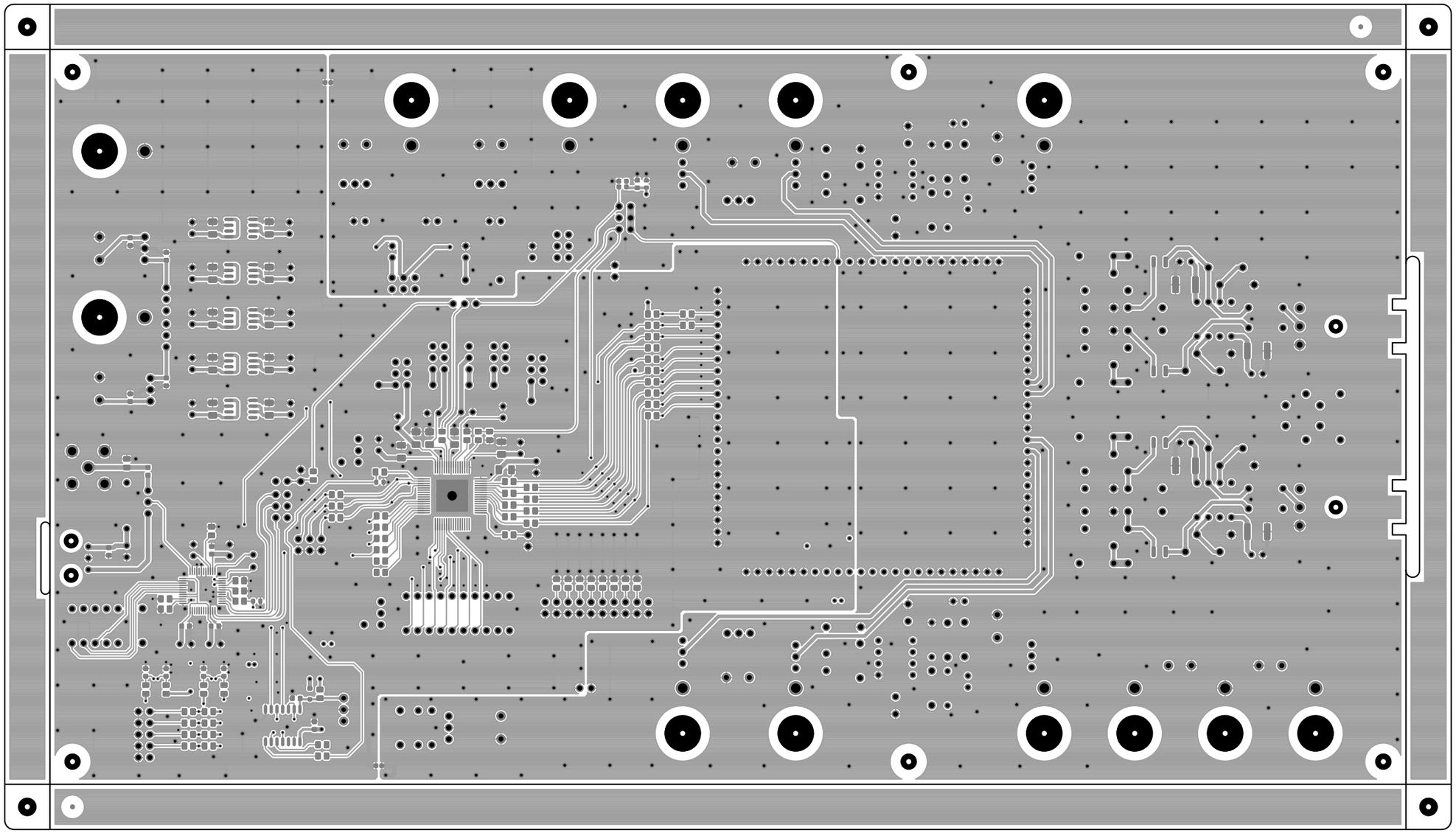
AKD449X-A-MAIN_Rev.0

半田面シルク図　　部品面透視図



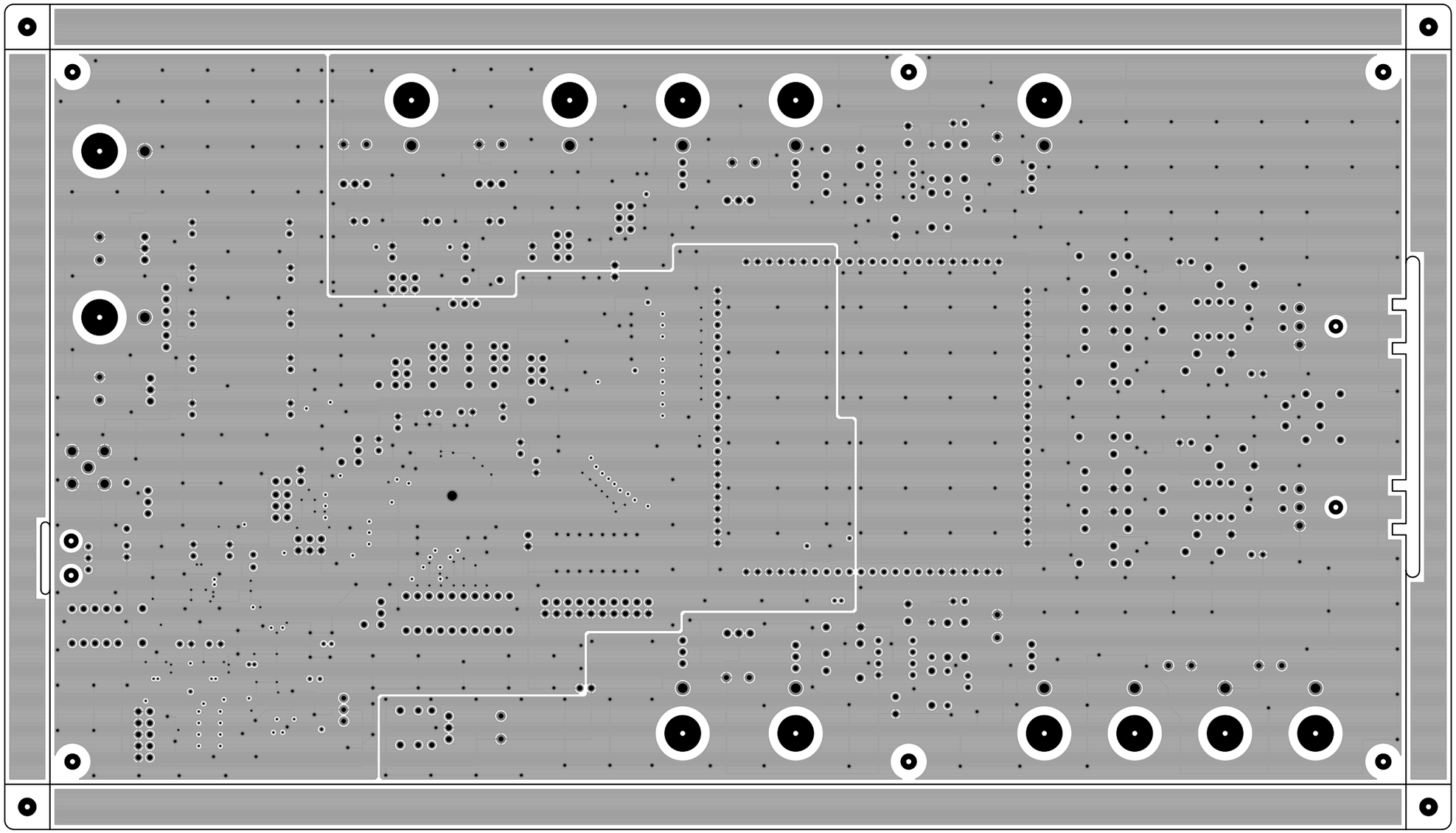
AKD449X-A-MAIN_Rev.0

部品面パターン図　　部品面透視図



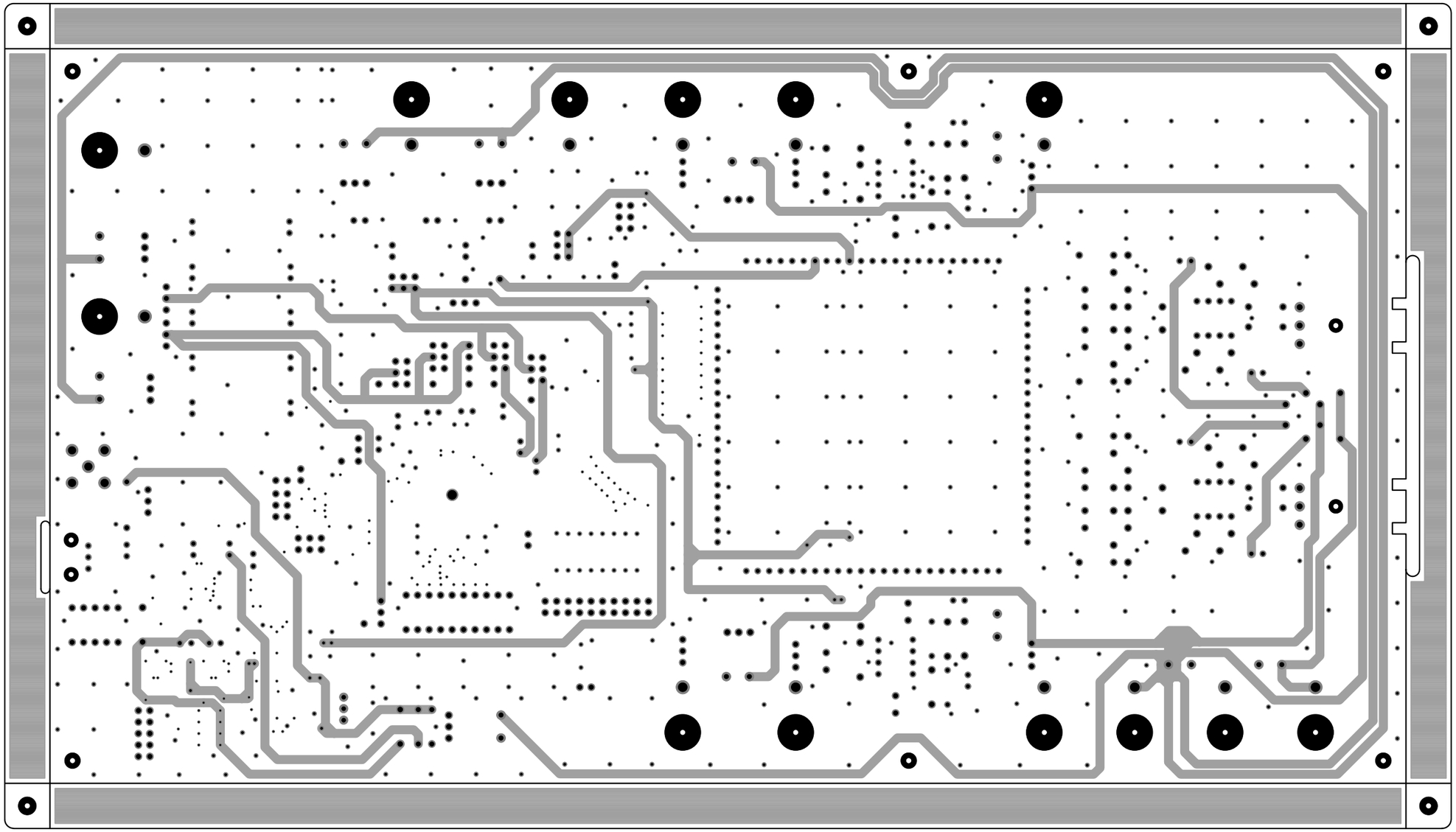
AKD449X-A-MAIN_Rev.0

内層Ｌ２パターン図　　部品面透視図



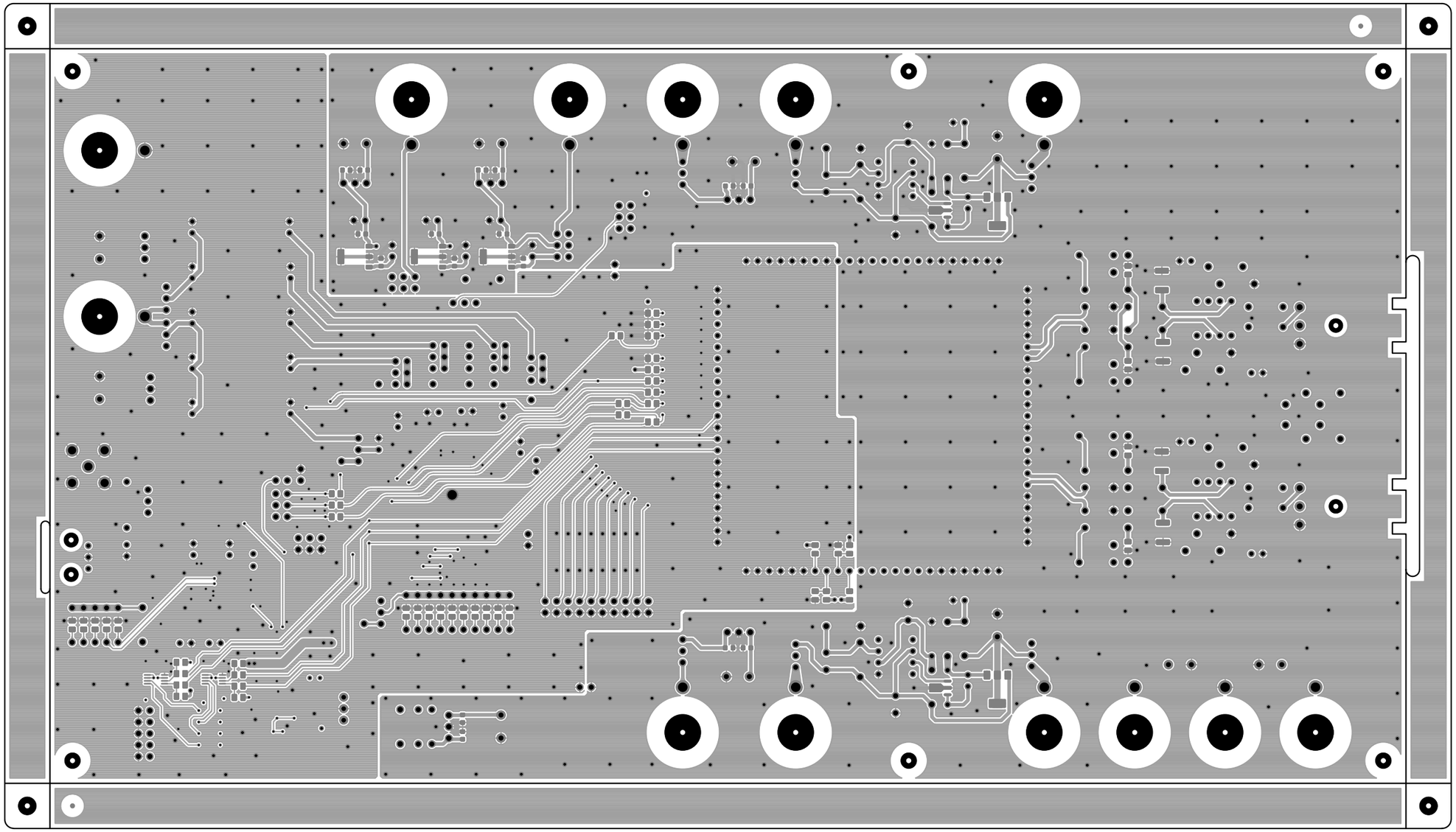
AKD449X-A-MAIN_Rev.0

内層L3パターン図　　部品面透視図



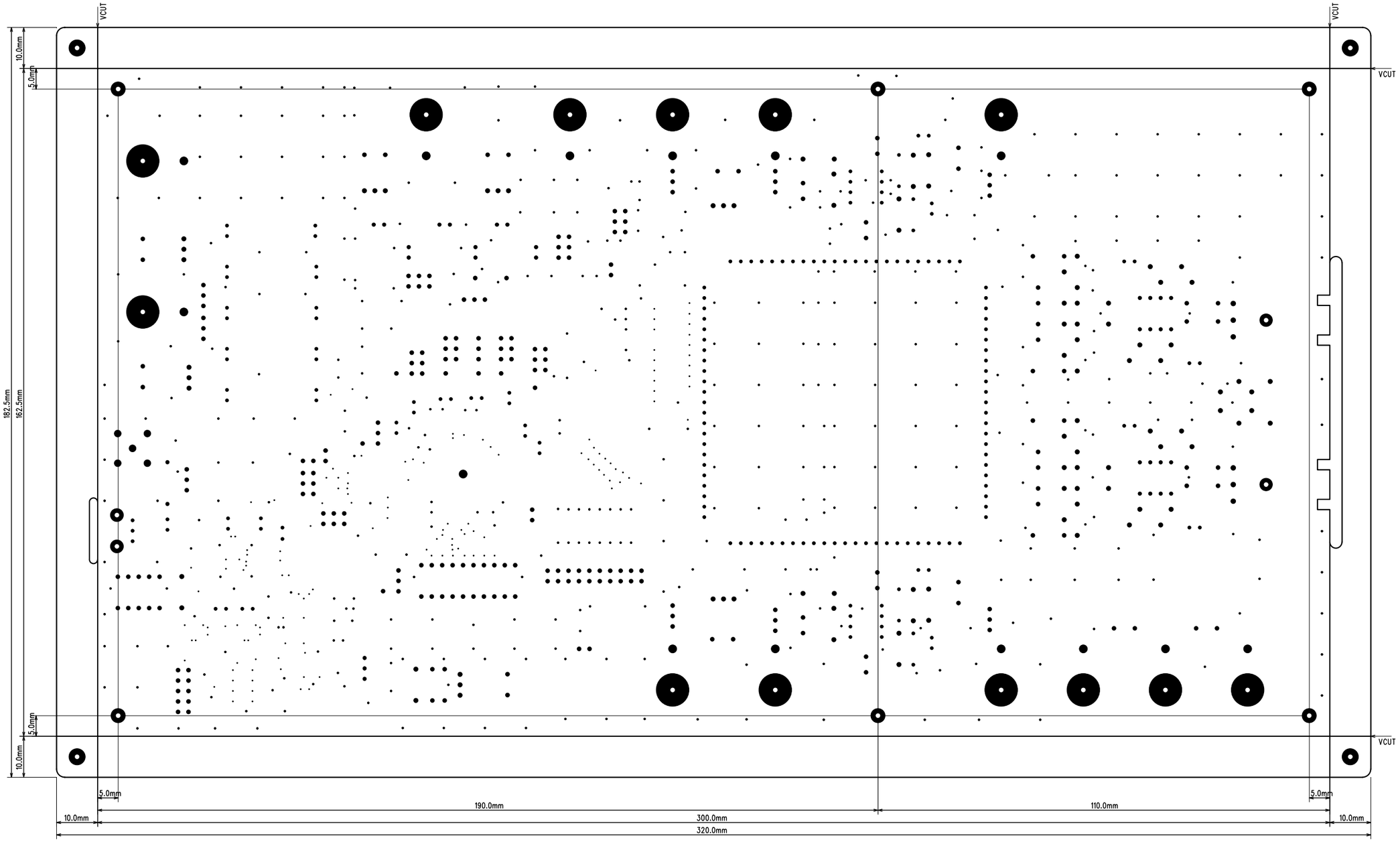
AKD449X-A-MAIN_Rev.0

半田面パターン図　　部品面透視図



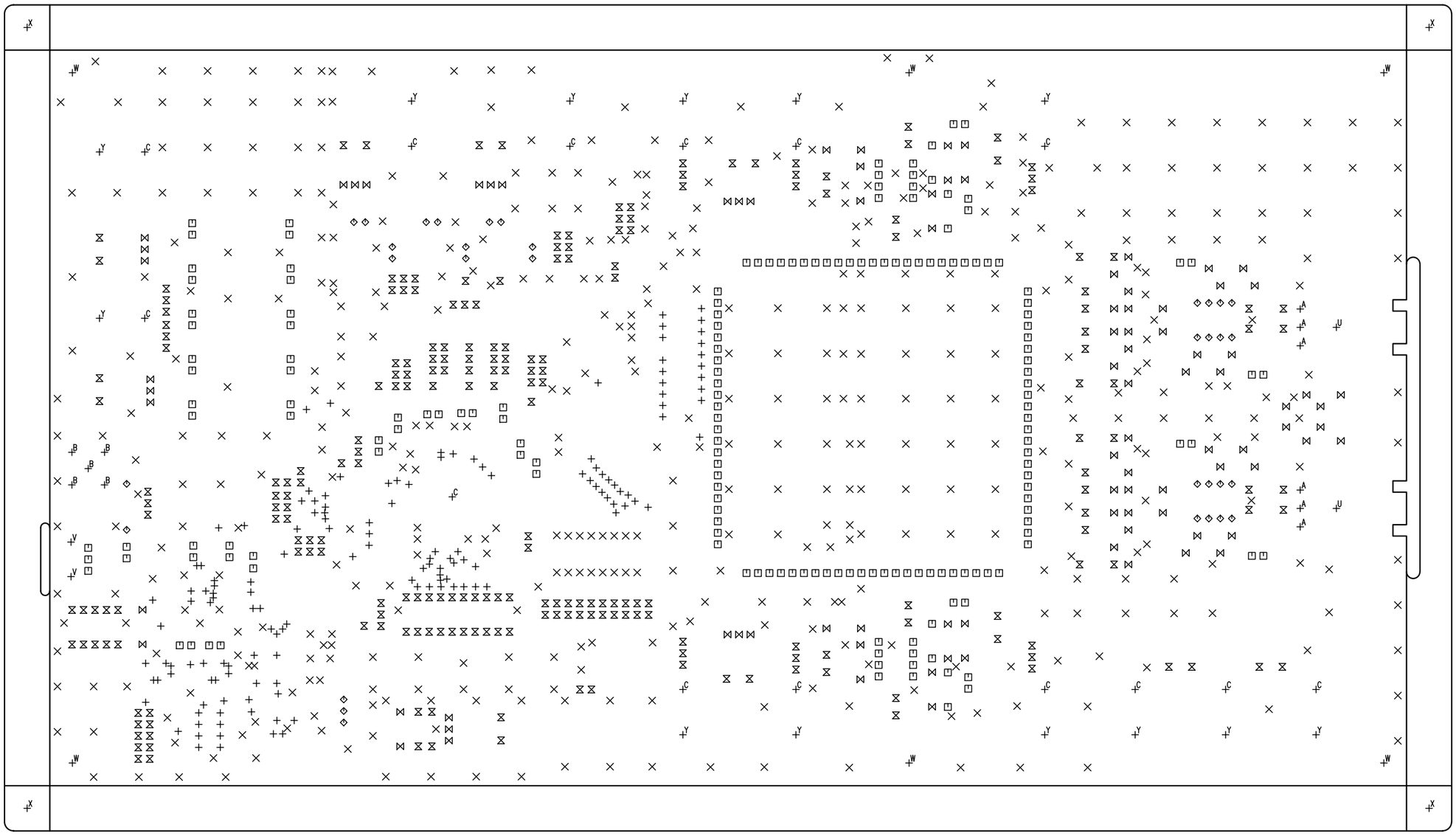
AKD449X-A-MAIN_Rev.0

外形図、寸法図　　部品面透視図



AKD449X-A-MAIN_Rev.0

穴径図　　部品面透視図



寸法	個数	記号	PLTD
0.3	144	+	PLTD
0.5	470	×	PLTD
0.8	181	□	PLTD
0.9	33	◇	PLTD
1	234	⧖	PLTD
1.1	93	⋈	PLTD
1.2	6	A	PLTD
1.7	5	B	PLTD
2	14	C	PLTD
3.1	2	U	NPLTD
3.2	2	V	NPLTD
3.5	6	W	NPLTD
4	4	X	NPLTD
8	13	Y	NPLTD

※　ＰＬＴＤはスルーホールです。
※　ＮＰＬＴＤはノンスルーホールです。
※　穴径は全て仕上がり径でお願いいたします。
※　指示なき穴径公差は±0.05mm

AKD449X-A-MAIN_Rev.0

部品面透視図