AsahiKASEI MICRODEVICES

AK4497S
Application Note

1. General Description

This Application Note is intended to assist in designing systems using the AK4497S.

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3. Acronyms

		Description
(1)	PCM	Pulse Code Modulation
(2)	DSD	Direct Stream Digital
(3)	FS	Sampling Frequency
(4)	FSB	Base Sampling Frequency (ex. FSB is 48 kHz when FS = 48, 96,192, 384, 768 or 1536 kHz.) (ex. FSB is 44.1 kHz when FS = 44.1, 88.2,176.4, 352.8, 705.6 or 1411.2 kHz.)

4. AK4497S Function List

Table 1 shows the functions available in PCM/EXDF/DSD modes.
In Pin Control mode, only a few functions are available. Refer to P38 in the datasheet for the functions available in Pin Control mode.

Table 1. Function List of PCM/EXDF/DSD mode @Register Control Mode
(Y: Available, N/A: Not available)

Function	Default State	Address	Register Name	PCM mode	EXDF mode	DSD mode	
						Normal	Volume Bypass
Automatic Conversion Mode Switching (PCM/DSD, EXDF/DSD)	Disable	15H	ADPE	Y	Y	Y	Y
Manual Conversion Mode Select (PCM, DSD, EXDF)	PCM mode	00H 02H	EXDF DP	Y	Y	Y	Y
DSD Path Select	Normal Path	06H	DSDD	N/A	N/A	Y	Y
System Clock Setting Mode Select @ PCM mode	Manual Setting Mode	00H	ACKS	Y	N/A	N/A	N/A
MCLK Frequency Select @ DSD mode	512fsb	02H	DCKS	N/A	N/A	Y	Y
WCK Frequency Select @ EXDF mode	768kHz	00H	ECS	N/A	Y	N/A	N/A
Digital Filter Select @ PCM mode	Short Delay Sharp Roll-off Filter	01H 02H 05H	SD SLOW SSLOW	Y (Note 1)	N/A	N/A	N/A
Digital Filter Select @ DSD mode	39 kHz Filter	09H	DSDF	N/A	N/A	Y	N/A
De-emphasis Response	OFF	01H	DEM[1:0]	Y	N/A	N/A	N/A
Audio Serial Data Interface Format Select @ PCM mode	32-bit MSB	00H	DIF[2:0]	Y	N/A	N/A	N/A
Audio Serial Data Interface Format Select @ EXDF mode	24-bit LSB	00H	DIF[2:0]	N/A	Y	N/A	N/A
TDM Interface Format Select	Normal mode	0AH	TDM[1:0]	Y	N/A	N/A	N/A
Daisy Chain	Normal mode	0BH	DCHAIN	Y	N/A	N/A	N/A
Digital Attenuator Attenuation Level Setting	0 dB	03-04H	ATTL[7:0] ATTR[7:0]	Y	Y	Y	N/A
Gain Control	2.8 Vpp	07H	GC[2:0]	Y	Y	Y	N/A
Zero Detection	Disable	01H	DZFE	Y	Y	Y	N/A

Inverting Polarity of DZFL/R pins	"H" at detecting zero	02H	DZFB	Y	Y	Y	Y
Mono/Stereo mode Select	Stereo	02H	MONO	Y	Y	Y	Y
Analog Output Polarity Invert	OFF	05H	INVL/R	Y	Y	Y	Y
Data Selection of L-channel and R-channel	Not Swap (Stereo) Rch (Mono)	02H	SELLR	Y	Y	Y	Y
Sound Quality Select	Setting 1 & Setting 3	08H	SC[2:0]	Y	Y	Y	Y
Noise Free DSD Mute Function when Full-Scale Data Input	Disable	06H	DDM	N/A	N/A	Y	Y
Soft Mute Enable	Not Muted	01H	SMUTE	Y	Y	Y	N/A
RSTN	Reset	00H	RSTN	Y	Y	Y	Y
Clock Synchronization Function	Enable	07H	SYNCE	Y	Y	N/A	N/A

Note 1. The digital filter is fixed to super slow roll-off filter in Oct Speed Mode and Hex Speed Mode.
Note 2. Available in Normal Speed Mode, Double Speed Mode and Quad Speed Mode.

5. Recommended States when Changing Clock Frequency or Pin/Register Setting

Power Down, Standby and Reset functions of the AK4497S are controlled by PDN pin, STBYN bit, MCLK and RSTN bit (Table 2)。

Table 2. Power Down, Standby, and Reset function (*: do not care)

State	PDN pin	MCLK Input	STBYN bit	RSTN bit	Analog Output
Power Down	L	*	*	*	Hi-Z
Standby	H	No	*	*	Hi-Z
	H	Yes	0	*	Hi-Z
Reset	H	Yes	1	0	VCML/R
Normal Operation	H	Yes	1	1	Signal output

This chapter describes which states the AK4497S should be in when changing clock frequency, control pin settings and register settings.

5.1. Clock Frequency

Table 3 shows the states that are allowed when changing the clock frequencies or are stopped.

Table 3. Permitted States When Changing Clock Frequencies
(Y: Permitted, N/A: Not Permitted)

Clock	Power Down	Standby	Reset	Normal Operation	Notes
MCLK frequency	Y	Y	Y	N/A	-
BICK frequency	Y	Y	Y	N/A	Note 3
LRCK frequency	Y	Y	Y	N/A	Note 3
DCLK frequency	Y	Y	Y	N/A	-

Note 3. When ACKS bit = “0” and AFSD bit = “0”, BICK and LRCK frequencies must be changed in the Standby or reset state. It is possible to change BICK and LRCK frequencies during normal operation when ACKS bit = “1” or AFSD bit = “1”, but click noise may occur. This click noise can be avoided by the external mute circuit.

MCLK must be provided at the frequency ratios shown in Table 4 and Table 5.
When using the AK4497S at the N/A frequency ratios, the internal operating frequency decreases, leading to deterioration in THD+N characteristics. Please use at the N/A frequency ratios at your own risk.

Table 4 System Clock Example 1 (Auto Setting mode @Pin Control mode)

LRCK	MCLK Frequency [MHz]						Sampling Speed Mode
fs	32fs	48fs	64fs	96fs	128fs	192fs	
32.0kHz	N/A	N/A	N/A	N/A	N/A	N/A	Normal (≤ 32kHz)
44.1kHz	N/A	N/A	N/A	N/A	N/A	N/A	Normal (> 32kHz)
48.0kHz	N/A	N/A	N/A	N/A	N/A	N/A	
88.2kHz	N/A	N/A	N/A	N/A	N/A	N/A	Double
96.0kHz	N/A	N/A	N/A	N/A	N/A	N/A	
176.4kHz	N/A	N/A	N/A	N/A	22.5792	33.8688	Quad
192.0kHz	N/A	N/A	N/A	N/A	24.5760	36.8640	
384kHz	N/A	N/A	24.576	36.864	N/A	N/A	Oct
768kHz	24.576	36.864	N/A	N/A	N/A	N/A	Hex

(N/A: Not available)

Table 5 System Clock Example 2 (Auto Setting mode @Pin Control mode)

LRCK	MCLK Frequency [MHz]						Sampling Speed Mode
fs	256fs	384fs	512fs	768fs	1024fs	1152fs	
32.0kHz	8.1920	12.2880	16.3840	24.5760	32.7680	36.8640	Normal (≤ 32kHz)
44.1kHz	11.2896	16.9344	22.5792	33.8688	N/A	N/A	Normal (> 32kHz)
48.0kHz	12.2880	18.4320	24.5760	36.8640	N/A	N/A	
88.2kHz	22.5792	33.8688	N/A	N/A	N/A	N/A	Double
96.0kHz	24.5760	36.8640	N/A	N/A	N/A	N/A	
176.4kHz	N/A	N/A	N/A	N/A	N/A	N/A	Quad
192.0kHz	N/A	N/A	N/A	N/A	N/A	N/A	
384kHz	N/A	N/A	N/A	N/A	N/A	N/A	Oct
768kHz	N/A	N/A	N/A	N/A	N/A	N/A	Hex

(N/A: Not available)

5.2. Control Pin Setting (Pin Control Mode)

Table 6 shows the states that are allowed when changing the pin settings in pin control mode.

Table 6 Permitted States When Changing Control Pin Settings (Pin Control Mode)
(Y: Permitted, N/A: Not Permitted)

Pin	Power Down	Standby	Normal Operation	Notes
TDM0/1	Y	Y	N/A	-
SMUTE	Y	Y	Y	-
DIF0/1/2	Y	Y	N/A	-
HLOAD	Y	Y	N/A	-
GAIN	Y	Y	N/A	-
DCHAIN	Y	Y	N/A	-
DEM0	Y	Y	Y	Note 4
INVR	Y	Y	Y	Note 4
SD, SLOW, SSLOW	Y	Y	N/A	Note 5 Note 6
ACKS	Y	Y	N/A	-

Note 4. When switching in the normal operation state, it is recommended to switch at zero-data input or soft-mute state by SMUTE pin = "H" in order to avoid click noise during switching.

Note 5. Click noise may occur when the digital filter setting is changed. If click noise can be avoided by the external mute circuit, digital filter setting can be changed during normal operation.

Note 6. When changing from the Super slow roll-off filter to any other filter or vice versa in normal operation, the latency may deviate from the expected value (see section 6.1). To avoid this, change setting of these pins in Power Down or Standby state.

5.3. Register Setting (Register Control Mode)

Table 7 shows the states that are allowed when changing register settings in register control mode.

Table 7 Permitted States When Changing Register Settings (Register Control Mode)
(Y: Permitted, N/A: Not Permitted)

Register	Standby	Reset	Normal Operation	Notes
DIF[2:0]	Y	Y	N/A	-
AFSD	Y	Y	N/A	-
ECS	Y	Y	N/A	-
EXDF	Y	Y	N/A	-
ACKS	Y	Y	N/A	-
SMUTE	Y	Y	Y	-
DEM[1:0]	Y	Y	Y	Note 7
DFS[2:0]	Y	Y	N/A	-
SD, SLOW, SSLOW	Y	Y	N/A	Note 8 Note 9
DZFE, DZFM	Y	Y	Y	
SELLR	Y	Y	Y	Note 7
DZFB	Y	Y	Y	-
MONO	Y	Y	Y	Note 7
DCKB	Y	Y	N/A	-
DCKS	Y	Y	N/A	-
DP	Y	Y	N/A	-
ATTL[7:0], ATTR[7:0]	Y	Y	Y	-
INVL, INVR	Y	Y	Y	Note 7
DSDSEL[1:0]	Y	Y	N/A	-
DSDD	Y	Y	N/A	-
DMC	Y	Y	N/A	-
DDM	Y	Y	N/A	-
SYNCE	Y	Y	N/A	-
GC[2:0]	Y	Y	N/A	
SC[2:0]	Y	Y	N/A	
HLOAD	Y	Y	N/A	
DSDF	Y	Y	Y	Note 7
DSDPATH	Y	Y	N/A	
SDS[2:0]	Y	Y	Y	Note 7
TDM[1:0]	Y	Y	N/A	-
DCHAIN	Y	Y	N/A	
ATS[1:0]	Y	Y	Y	Note 10

Note 7. When switching in the normal operation state, it is recommended to switch at zero-data input or soft-mute state by SMUTE bit = "1" in order to avoid click noise during switching.

Note 8. Click noise may occur when the digital filter setting is changed. If click noise can be avoided by the external mute circuit, digital filter setting can be changed during normal operation.

Note 9. When changing from the Super slow roll-off filter to any other filter or vice versa in normal operation, the latency may deviate from the expected value (see section 6.1). To avoid this, change setting of these bits in Standby or Reset state.

Note 10. Do not change the ATS[1:0] bits while operating gain transition by SMUTE bit, ATTL[7:0] bits and ATTR[7:0] bits switching.

6. Latency in Each Playback Mode

Latency is the internal processing time it takes for the input digital data to be output as an analog signal.

6.1. PCM mode

Latency in PCM mode is the time from when the impulse data is set in the input register until the peak of the analog signal is output (Figure 1). The latency at PCM mode is the sum of the digital filter group delay and the other operational delays shown below.

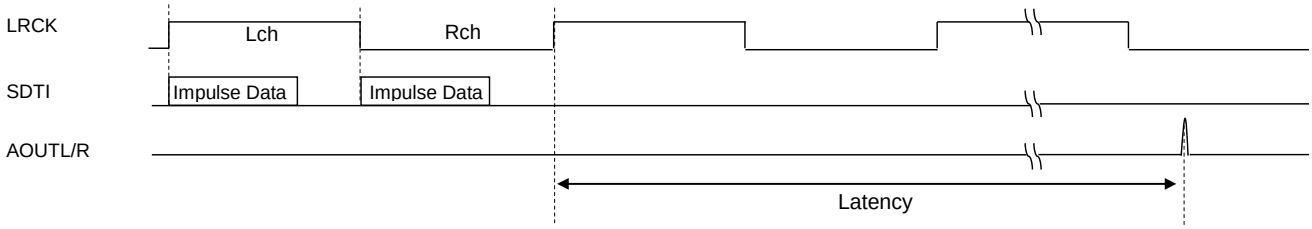


Figure 1. PCM mode Latency

In PCM mode, group delays such as Table 8 occur according to the settings of the digital filter.

Table 8 Group Delay (PCM mode)

SSLOW bit	SD bit	SLOW bit	Mode	Group Delay (Note 11)	
0	0	0	Sharp roll-off filter	29.2/fs	
0	0	1	Slow roll-off filter	6.5/fs	
0	1	0	Short delay sharp roll-off filter	6.0/fs	(default)
0	1	1	Short delay slow roll-off filter	5.0/fs	
1	0	0	Super slow roll-off filter	0.6/fs–2.5/fs (Note 12)	
1	0	1			
1	1	0	Low dispersion short delay filter	10/fs	
1	1	1	N/A	N/A	

Note 11. When the AK4497S is in Oct Speed Mode or Hex Speed Mode, Super Slow roll-off filter is selected regardless of SSLOW/SD/SLOW bit setting.

Note 12. 0.6/fs in Normal Speed Mode. It varies in the range of 0.6/fs-2.5/fs depending on the Sampling Speed setting.

In addition, in PCM mode, there is a delay error due to the timing of capturing data at the data interface. The delay error depends on the Synchronization Function (SYNCE bit) setting (Table 9).

Table 9 Delay Error at the Data Interface (PCM mode)

SYNCE bit	Delay Error	
0	<±1/fs	
1	<±0.3 μs	(default)

(e.g.) Latency when PCM mode, fs = 44.1 kHz, Sharp Roll-off filter and SYNCE bit = “0”.

Latency = (29.2 ± 1)/fs = 662 ± 23 μs

6.2. DSD mode

Latency in DSD mode is approximately 8 μs in DSD64 mode, which varies slightly depending on the operation rate and DSDF bit.

7. Design of Analog Output Post-Circuit

7.1. Calculation of the DC load resistance

The external circuit after the analog output pins (AOUTP, AOUTN) must be designed so that its DC load resistance (R_L) complies with the "Load Resistance" specifications given in chapter 8 in the datasheet. The R_L is the effective resistance between the analog output pins and the system analog ground (Figure 2). This section describes how to calculate the DC load resistance by referring to the circuit as shown in Figure 3.

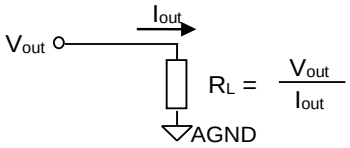


Figure 2. Schematic Diagram of the R_L

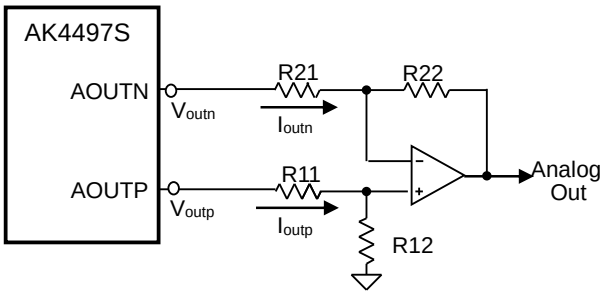


Figure 3. Example of Differential-to-Single Circuit

The R_L is determined by $R_L = V_a/I_a$ from I_a at full-scale current output and output voltage V_a of AOUTx pin (Figure 4). For normal operation of the AK4497S, both the R_{Lp} (R_L of AOUTP pin) and the R_{Ln} (R_L of AOUTN pin) must satisfy the specification ($R_L \geq 120\ \Omega$, HLOAD bit = "1").

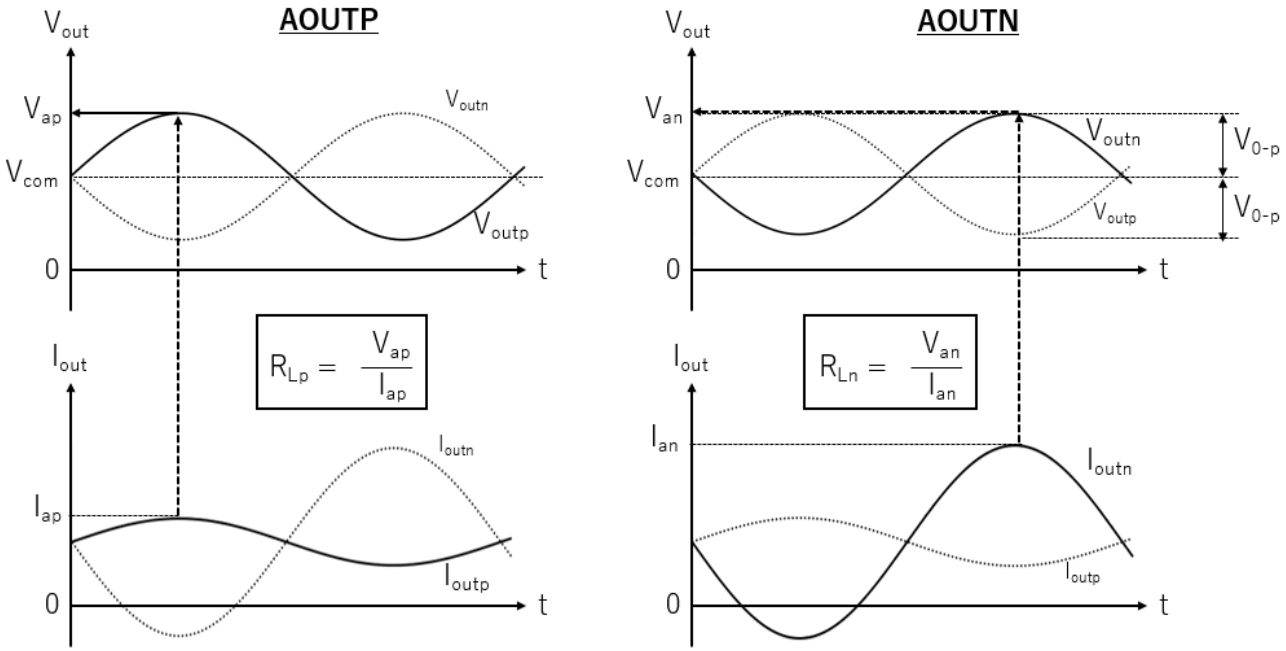


Figure 4. R_{Lp} and R_{Ln} in the Figure 4 Schematic

In Figure 3 case, the R_{Lp} and the R_{Ln} are,

$$R_{Lp} = \frac{V_{ap}}{I_{ap}} = R_{11} + R_{12}$$

$$R_{Ln} = \frac{V_{an}}{I_{an}} = \frac{(V_{com} + V_{0-p})(R_{11} + R_{12})R_{21}}{R_{11}V_{com} + (R_{11} + 2R_{12})V_{0-p}}$$

Where,

$$V_{COM} = 0.5(VREFH - VREFL)$$

$$V_{0-p} = 0.28(VREFH - VREFL)$$

7.2. Filter Design

The formula for calculating the parameters of the second-order low-pass filter shown in Figure 5 is shown below.

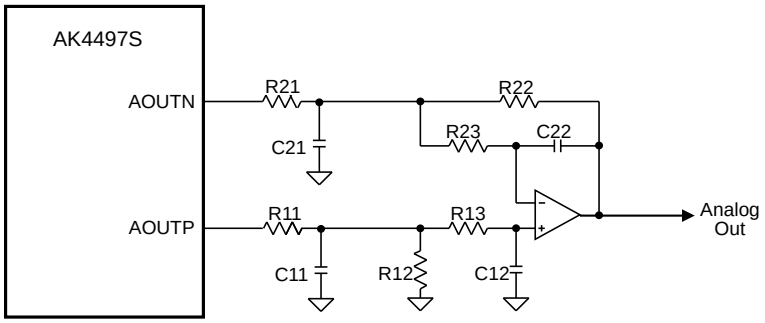


Figure 5. Second-Order Low-Pass Filter Circuit Example

$$DC\ Gain = \frac{0.5(R_{21}R_{12} + R_{11}R_{22}) + R_{12}R_{22}}{R_{21}(R_{11} + R_{12})}$$

$$f_{cp} = \frac{\omega_{0p}}{2\pi} \quad , \quad f_{cn} = \frac{\omega_{0n}}{2\pi}$$

$$\omega_{0p} = \frac{1}{\sqrt{C_{11}C_{12}R_{12}R_{13}}} \quad , \quad \omega_{0n} = \frac{1}{\sqrt{C_{21}C_{22}R_{22}R_{23}}}$$

$$Q_p = \frac{C_{11}\omega_{0p}}{\frac{1}{R_{11}} + \frac{1}{R_{12}} + \frac{1}{R_{13}}} \quad , \quad Q_n = \frac{C_{21}\omega_{0n}}{\frac{1}{R_{21}} + \frac{1}{R_{22}} + \frac{1}{R_{23}}}$$

$$R_{Lp} = \frac{V_{ap}}{I_{ap}} = R_{11} + R_{12}$$

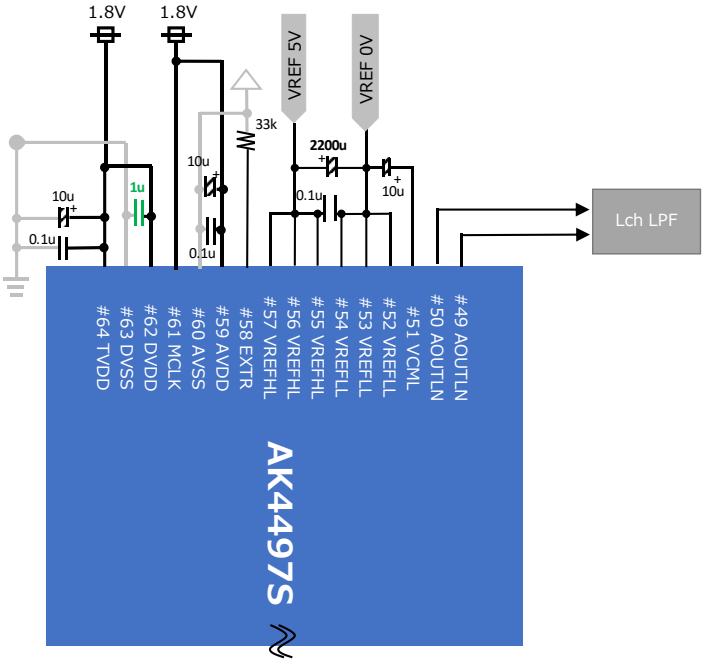
$$R_{Ln} = \frac{V_{an}}{I_{an}} = \frac{(V_{com} + V_{0-p})(R_{11} + R_{12})R_{21}}{R_{11}V_{com} + (R_{11} + 2R_{12})V_{0-p}}$$

8. Recommended Components

8.1. Capacitance Values to be noted

When LDOE = H, it is necessary to place a capacitor of **1 µF** between DVSS pin and DVDD pin (Figure 6). If the capacitance is higher than 1 µF, the internal circuit will not start up, and AK4497S will not operate. Conversely, if the capacitance is lower than 1 µF, the product will operate, but the power supply circuit in the AK4497S will be unstable, leading to unreliable circuit operation.

Figure 6 Part of the external circuit around AK4497S



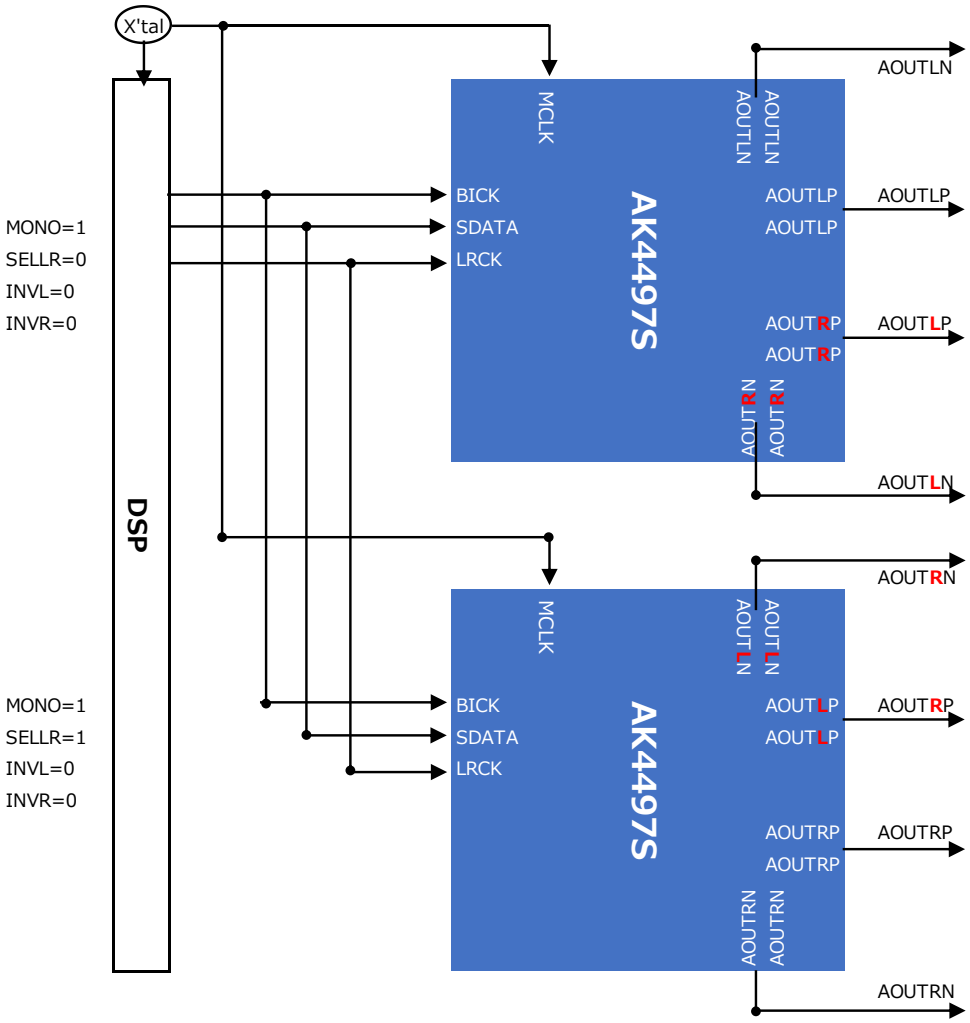
9. Device Connection Example in Dual Mono mode

In Register Control mode, AK4497S can be used in Dual Mono mode. Please refer to the settings in Table 10. Do not change the settings while SDATA or all clock signals are being input, such as during sound playback.

Table 10 Register setting Matrix in Dual Mono mode

AK4497S	MONO bit	SELLR bit	INVL bit	INVR bit		AOUTLN	AOUTLP	AOUTRP	AOUTRN
for Lch	1	0	0	0		LN	LP	LP	LN
	1	0	0	1		LN	LP	LN	LP
	1	0	1	0		LP	LN	LP	LN
	1	0	1	1	→	LP	LN	LN	LP
for Rch	1	1	0	0		RN	RP	RP	RN
	1	1	0	1		RN	RP	RN	RP
	1	1	1	0		RP	RN	RP	RN
	1	1	1	1		RP	RN	RN	RP

Figure 7 Connection example in Dual Mono mode



10. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
25/04	00	First Edition	-	-

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