AN1093: Achieving Low Jitter Using an Oscillator Reference with the Si5342-47 Jitter Attenuators

This applican note references the Si5342-7 jitter attenuator products that use an oscillator as the frequency reference connected to the XA/XB input. Although many types of oscillators can be used with the Si5342-47, a common use case is when a TCXO/OCXO is needed to meet the requirements of Synchronous Ethernet (SyncE), G.8262, and other non-SyncE applications that use a low PLL bandwidth.

Additionally, this application note describes how to achieve low jitter using an oscillator as the reference on the XA/XB pins, methods for selecting the TCXO/OCXO, and the importance of layout. This application note also describes attenuator design, including circuit recommendations for various TCXO outputs, and how these outputs can affect rise times, fall times, and input signal swing.

A noise comparison is also provided in which two different input power supplies use varying bypass capacitors going into two different TCXOs. This comparison shows the jitter performance going into the Si534x device as well as the output performance from the Si5344H. Finally, the differences between using an OCXO in place of a TCXO are defined.

In order to meet the wander generation and attenuation limits in G.8262, the Si534x DSPLL loop BW must be below 10 Hz. The standard configuration of the Si534x uses a crystal (see Figure 1.1 Crystal Resonator Connection on page 2) but the wander characteristics of an uncompensated crystal will result in not meeting some of the G.8262 requirements. A TCXO or OCXO has better wander stability than a crystal, and using a TCXO at the XA/XB pins will allow the device to meet the wander requirements outlined in ITU-T G.8262 (07/2010) section 8.1 (on wander generation) and section 10 (on wander transfer). This application note applies specifically to the Si5342-47 family of jitter attenuators. It does not apply to the Si5348 or the Si5383 because their TCXO/OCXOs are connected to the REF clock input pins, not the XA pin. Similarly, because a TCXO can be connected to its clock input pins, this application note is not relevant to the Si5340/41 clock generators.

Refer to *Si5345-Si5344-Si5342_Synchronous Ethernet-G.8262_ComplianceTest Results* for G.8262 details. The application note, "AN905: Si534X External References; Optimizing Performance" and reference manual "Si534x/8x Jitter Attenuators Recommended Crystal, TCXO and OCXO Reference Manual" are companion documents that list recommended circuits, vendors, and part numbers that provide complementary information on this subject.

KEY POINTS

- PCB layout for TCXOs is critical for low jitter
- A 3.3 V CMOS TCXO signal must be attenuated before it is applied to the XA pin
- For best performance, TCXOs require very clean power supplies

1. Selecting a TCXO to Connect to the XA/XB Pins

Designs that do not require a low loop bandwidth may benefit from using a standard crystal oscillator connected to the XA/XB pins instead of a crystal. This may be due to the fact that the oscillator output is already available on the PCB from an existing clock buffer, or it may be because the crystal oscillator is part of a list of approved vendor part numbers. See the figure below for connecting a standard crystal to a Si534x device.

With a loop BW below ~40 Hz, the use of a crystal for the XA/XB jitter reference becomes a problem because the wander of an uncompensated crystal affects low-offset phase noise. As a result, the PLL cannot meet the G.8262 requirements. Using a TCXO or OCXO delivers better wander stability. However, the TCXO must be chosen carefully by referring to the list of TCXO recommendations in the Si534x/8x Jitter Attenuators Recommended Crystal, TCXO and OCXO Reference Manual.

Oscillators usually come with two output options: clipped sine wave and CMOS. Oscillators with clipped sine wave outputs should be avoided because they have slow rise times that lead to increased jitter at the Si5342-47 XA/XB input. Because there is no jitter attenuation below 1 MHz from the XA/XB pins to the clock outputs, most of the jitter on the XA/XB pins will appear on the clock outputs of the Si5342-47. It is therefore important to select a low-jitter oscillator with reasonable output slew rates.

After selecting an appropriate oscillator, there are still other challenges. Oscillators with a single-ended output should be connected to the XA pin on the Si5342-47. However the oscillator signal must be attenuated from the standard 3.3V CMOS output to match the XA pin which has a maximum input swing of 2 V, pk-pk. Other issues like DC loading, PCB layout, and power supply sensitivity must also be considered to ensure optimal operation.

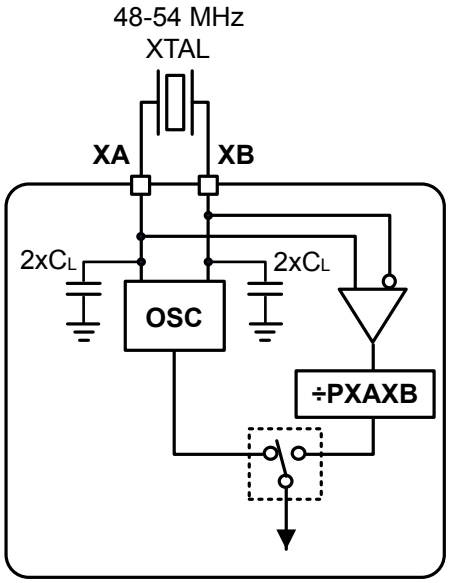

Figure 1.1. Crystal Resonator Connection

2. PCB Layout

The output drive capability of an oscillator must be considered when connecting it to the XA/XB pins. For example, a typical TCXO is specified with a load of 10 kΩ in parallel with 10 pf and can drive only 4 mA of output current. This puts constraints on both the attenuator (necessitated by the 2 V pk-pk swing at the XA input) and the PCB etch run. Because the attenuator will not have a high impedance and source termination will only work if the transmission ends at a high impedance, source termination at the TCXOs output is not particularly useful. Since a TCXO is unable to drive a 50 Ω end terminated load (either AC or DC coupled), the etch trace transmission line connecting the two cannot be terminated properly. To avoid signal integrity issues, the TCXO must be placed as close to the XA pin as possible so that the PCB etch transmission line will not need to be terminated.

3. Attenuator Design

The simplest approach to applying an attenuator from an oscillator such as a TCXO to the Si534x is shown below:

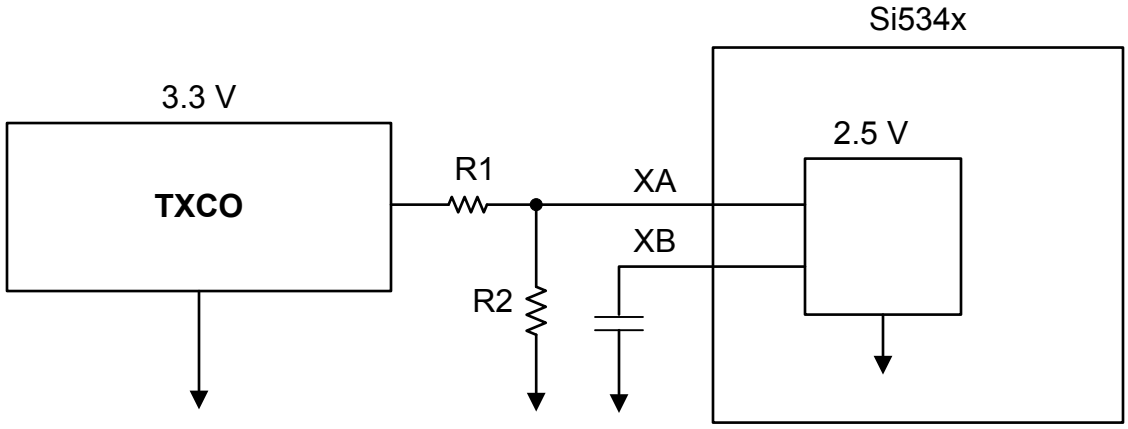

Figure 3.1. Simple Attenuator

There are, however, two issues with this circuit. The first issue is that the DC load that the oscillator sees is referenced to ground. A load that is centered at the halfway point (1.65V = 3.3V/2) will minimize the peak current coming out of the oscillator. The second issue is that the attenuator circuit acts as a low pass filter. If we assume that R1 = R2 = 5 kΩ so that the total DC load that the TCXO sees is 10 kΩ, the 10 pf input capacitance of the XA pin will create a low pass filter with a -3dB cutoff frequency of about 6.45 MHz = 1 / (2pi*R*C). With a 50 MHz oscillator frequency, the input signal pk-pk swing will be too small. Decreasing the value of R1 and R2 to increase the cutoff frequency will put too much of a DC load on the oscillator.

The recommended attenuation circuit is shown below:

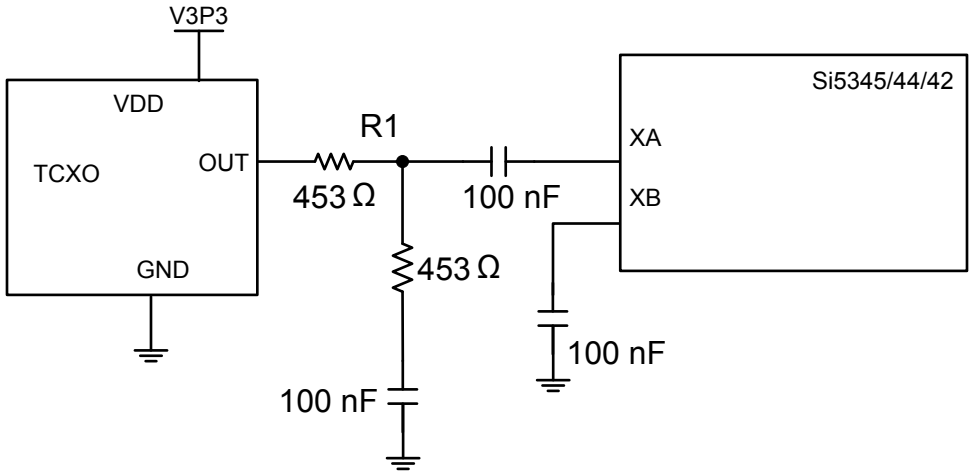

Figure 3.2. Recommended Oscillator to Si534x Attenuator

The low pass filter now has a cutoff frequency of ~70 MHz. With an oscillator frequency of 50 MHz, the fundamental will pass through and the third overtone will be attenuated, which is acceptable. Also, the load is centered at the average value of the oscillator's output. Here is a scope plot of the XA pin with the above circuit:

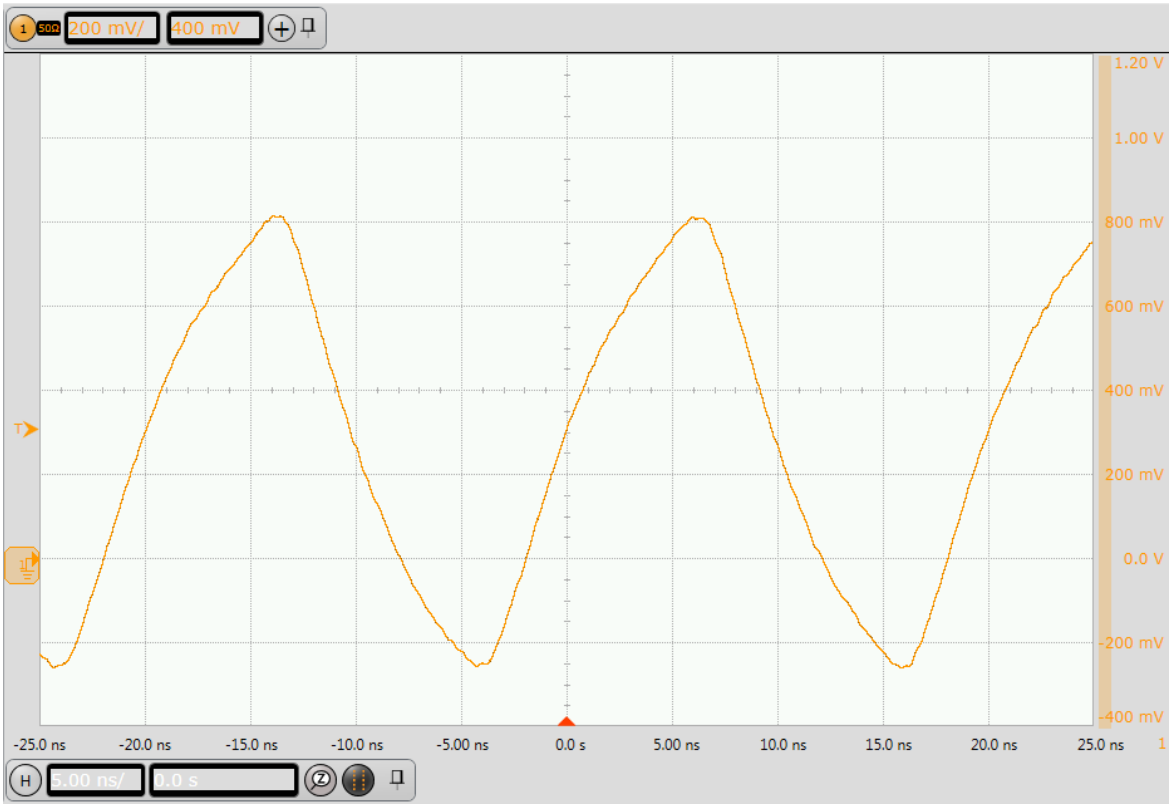

Figure 3.3. RC Attenuator Waveform

The slow rise time shown in the figure above makes the Si534x sensitive to noise when the signal crosses the threshold voltage of 1.2 V. For this reason, it is necessary to keep the oscillator as close to the Si534x as possible to minimize stray pickup.

Another unconventional approach to attenuation that uses capacitors is shown in the following schematic:

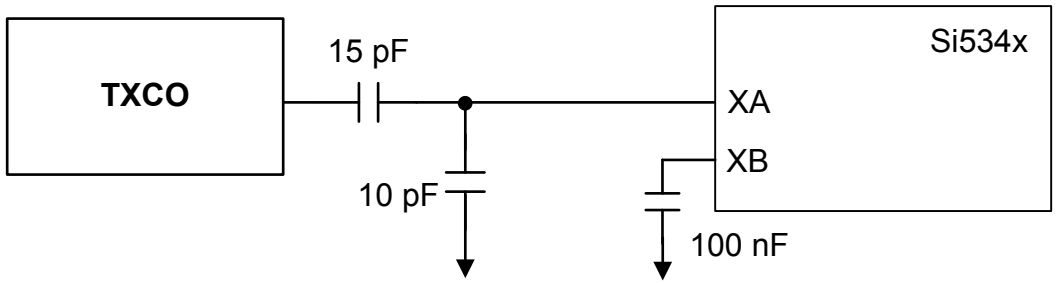

Figure 3.4. Capacitor Attenuator

The ratio of the capacitors determines the amount of attenuation and the series combination of the two provides the 10 pf load. The advantage of this circuit is that it provides better rise and fall times because it attenuates the harmonics of the 40 MHz signal less than the above RC attenuator. Figure 3.5 Capacitor Attenuator Waveform on page 6 shows the improved rise/fall time of the capacitor attenuator.

Figure 3.5. Capacitor Attenuator Waveform

4. Power Supply Noise

A very clean power supply is required to achieve superior jitter performance with an oscillator. To measure the effects of power supply noise, two TCXOs were mounted on a small evaluation board, pictured below:

Figure 4.1. TCXO Eval Board Picture

This evaluation board has a single 100 nf bypass cap and was powered by an Agilent model E3648A lab supply. Two representative TCXOs (labeled A and B) were used to generate the following phase noise plots. With this setup, TCXO A had the following phase noise plot:

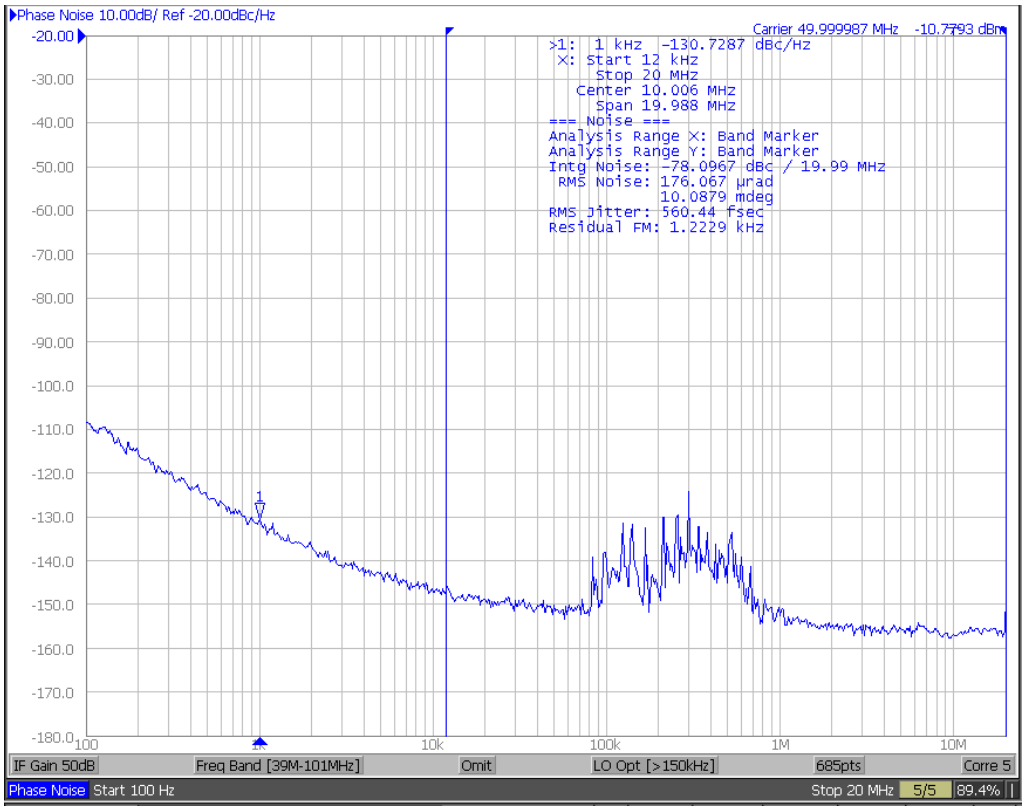

Figure 4.2. TCXO A with 100 nf

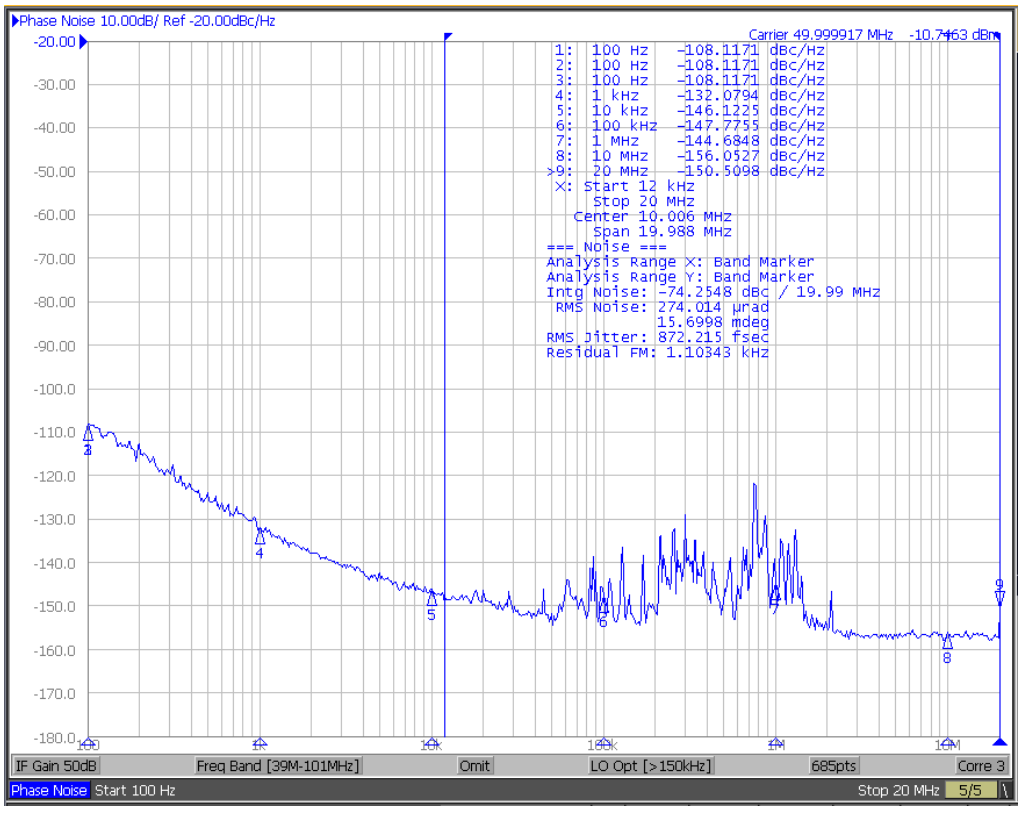

Figure 4.3. TCXO B with 100 nf

Both of these TCXO plots show a pronounced clump of spurs in the mid band. The signals from the A and B TCXOs were then used as the XA signals for an Si5344H eval board with an output frequency of 2.105 GHz.

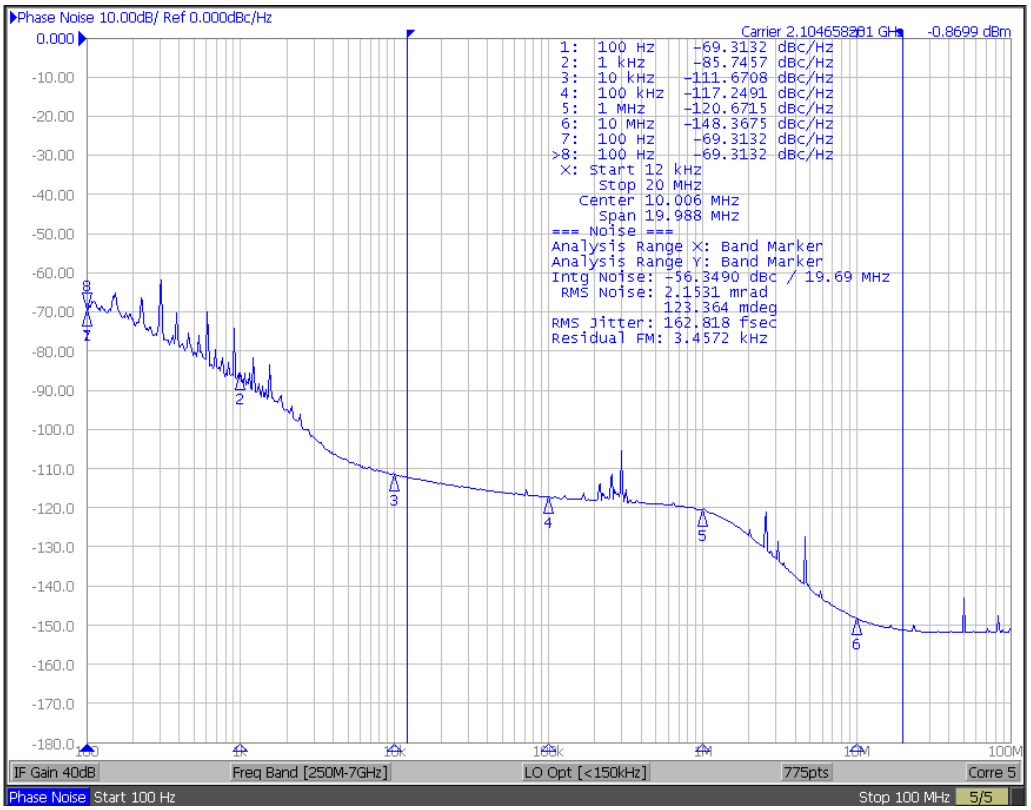

Figure 4.4. Si5344H with TCXO A and a 100 nf Cap

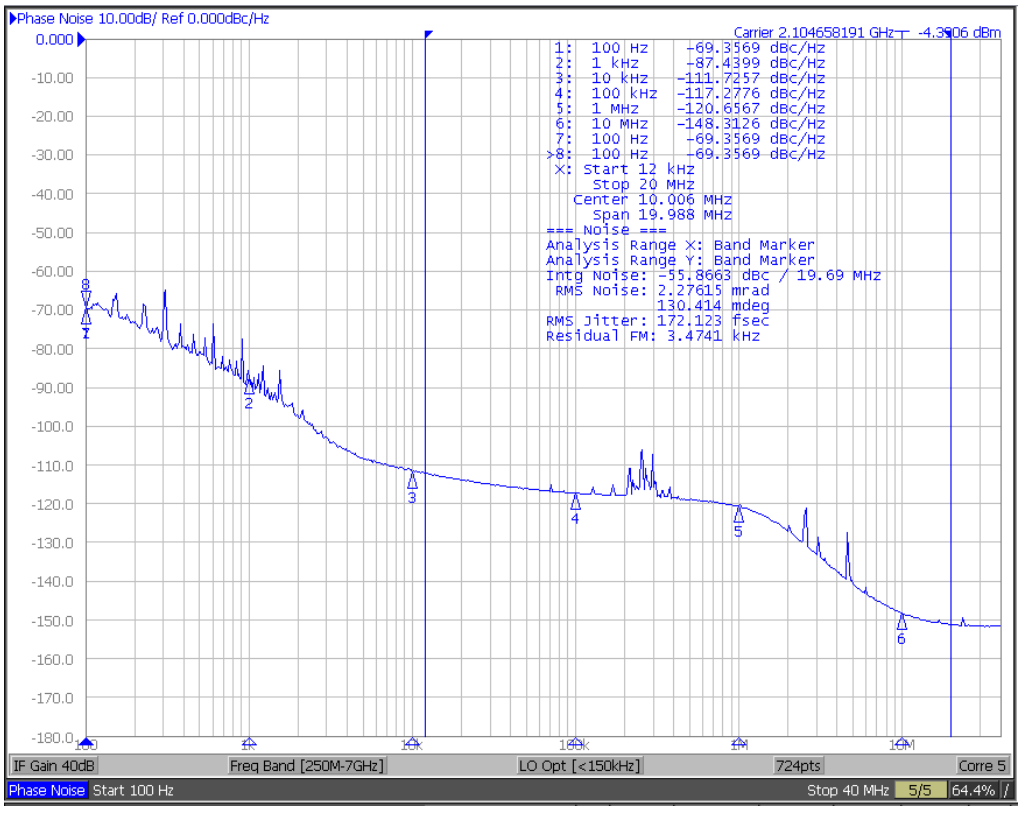

Figure 4.5. Si5344H with TCXO B and a 100 nf Cap

5. Power Supply Phase Noise Plot with Added 100 µF Bypass Cap

A 100 µF cap was added in parallel with the 100 nf bypass cap to both of the small TCXO eval boards and the above four plots were retaken. The resulting phase noise plots are as follows:

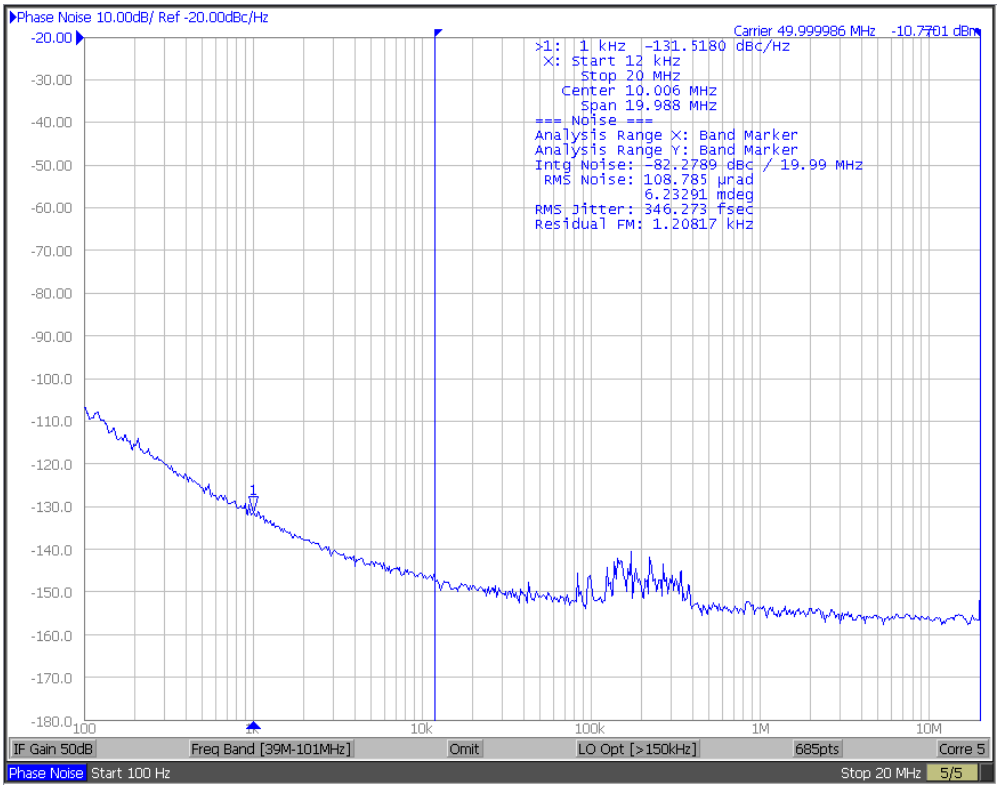

Figure 5.1. TCXO A with Added 100 µf Cap

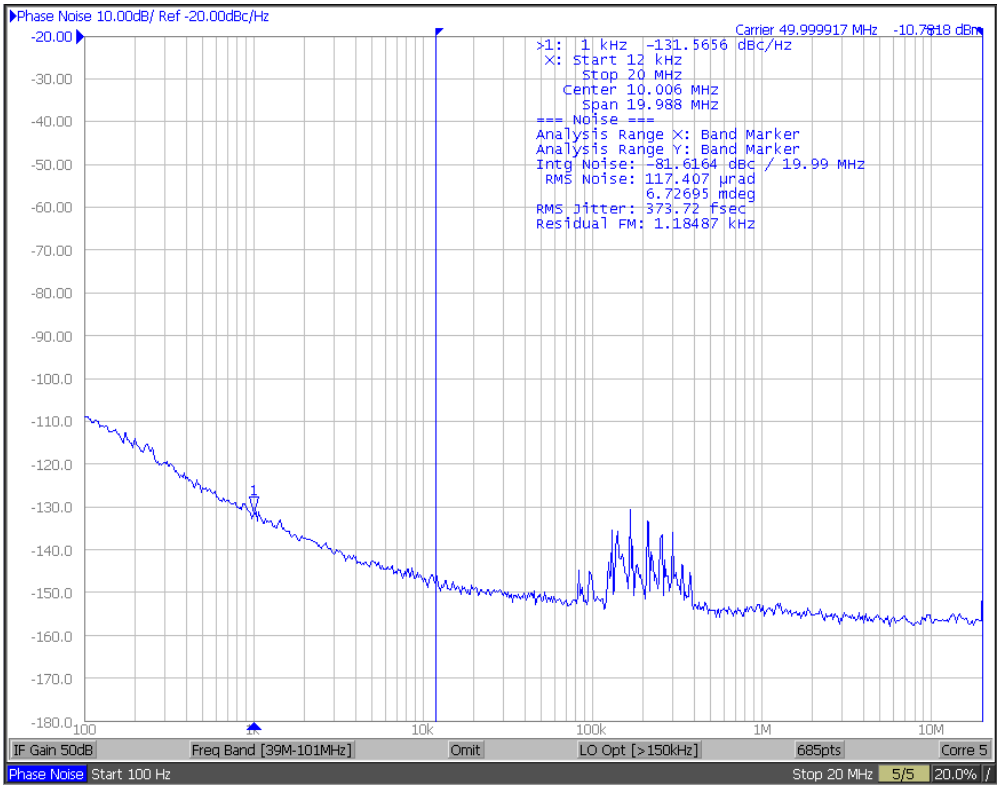

Figure 5.2. TCXO B with Added 100 µf Cap

As shown in Figure 5.1 TCXO A with Added 100 µf Cap on page 10 and Figure 5.2 TCXO B with Added 100 µf Cap on page 10, adding the 100 µF bypass cap significantly decreased the mid band phase noise, but did not eliminate it. These clock signals were used as the XA signal for the same Si5344H project file with the following results.

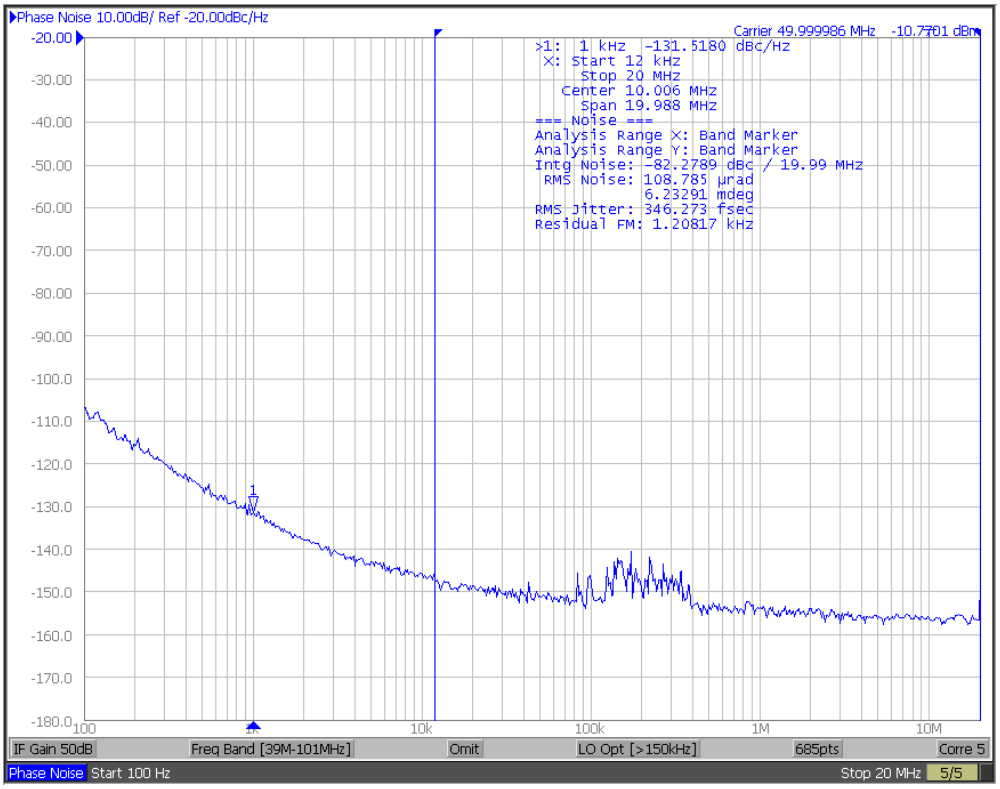

Figure 5.3. Si5344H using TCXO A with Added 100 µf Cap

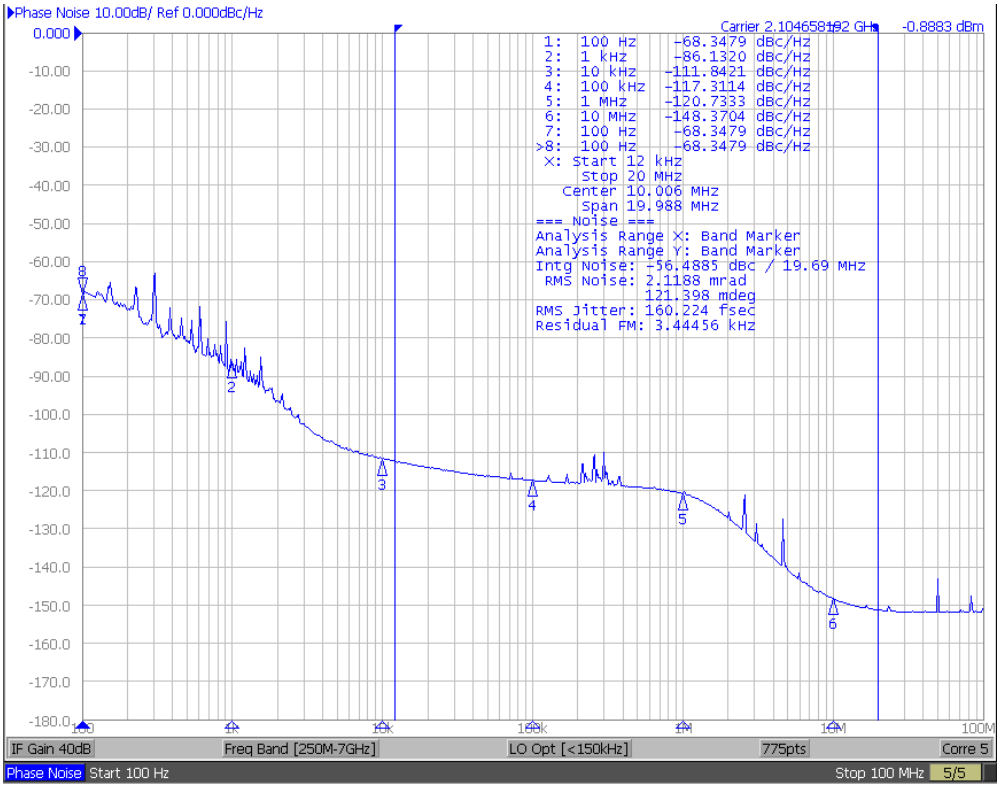

Figure 5.4. Si5344H using TCXO B with Added 100 µf Cap

The addition of the 100 µf bypass cap can improve performance, but there are still remnants of the mid band clump of spurs.

6. Using a Cleaner Power Supply

The next step to get improved jitter performance was to use a cleaner power supply going into the TCXO. The Keysight E5052B Source Signal Analyzer was used to power the small TCXO eval boards and the plots were repeated (using both the 100uF and the 100nF bypass caps).

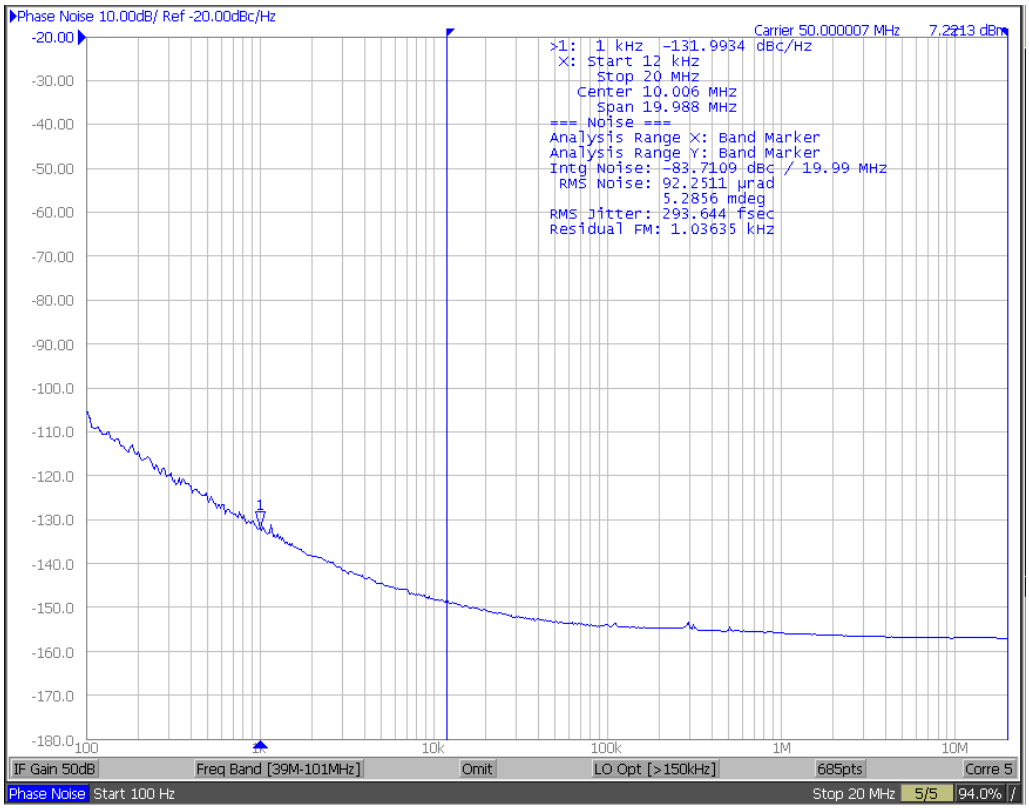

Figure 6.1. TCXO A using the E5052B Power Supply

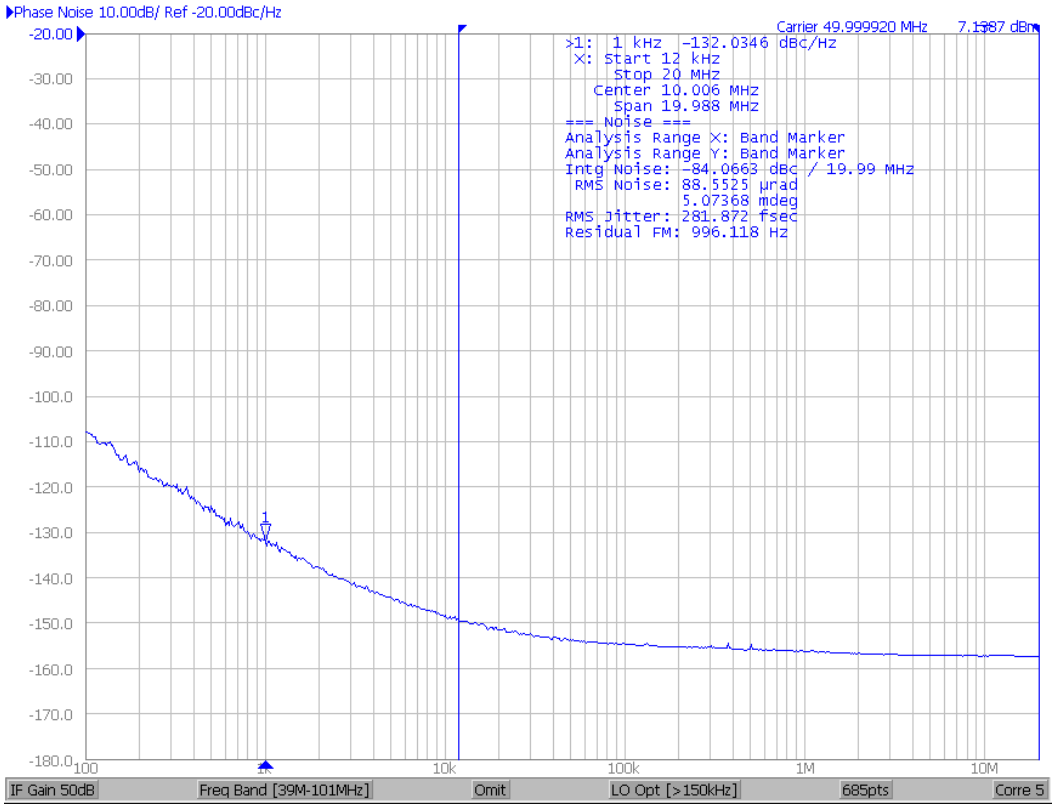

Figure 6.2. TCXO B using the E5052B Power Supply

The spurs have almost completely been eliminated and the XA clock source is finally clean. These two clock signals were then connected to the XA pin of the Si5344H eval board and plots were taken.

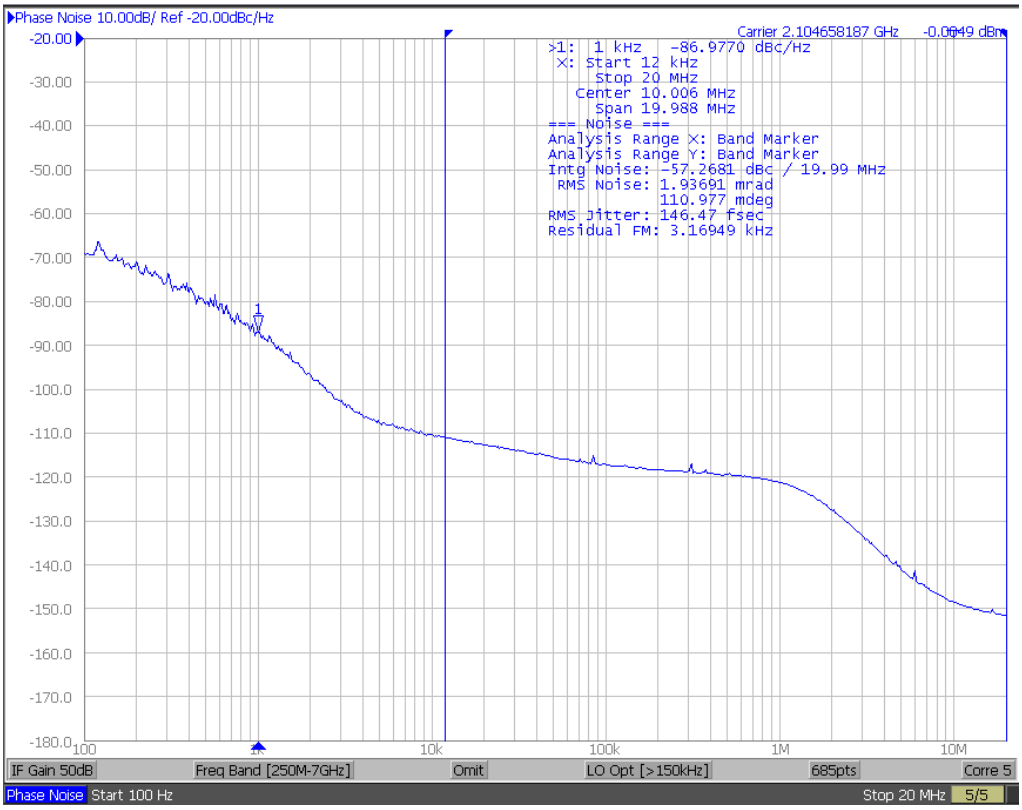

Figure 6.3. Si5344H with TCXO A and the E5052B Power Supply

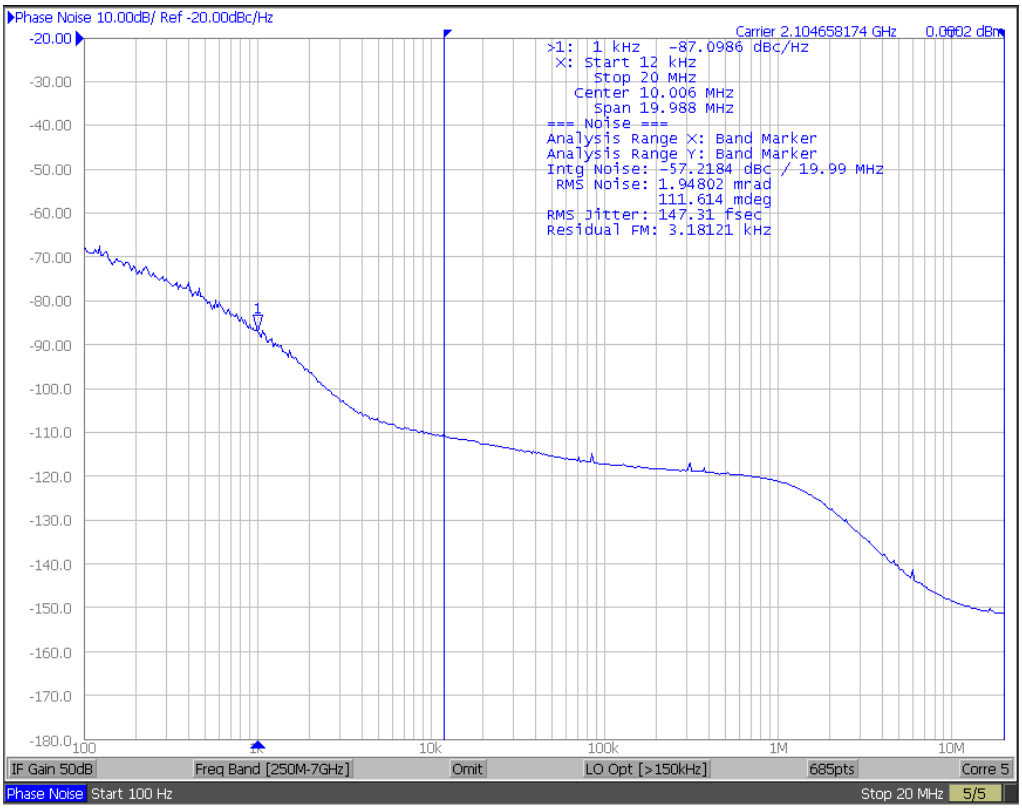

Figure 6.4. Si5344H with TCXO B and the E5052B Power Supply

Figure 6.3 Si5344H with TCXO A and the E5052B Power Supply on page 13 and Figure 6.4 Si5344H with TCXO B and the E5052B Power Supply on page 14 show improved jitter.

7. Using a High Performance OCXO

As an indication of Si5344H performance with a very clean XA/XB source, a high performance (and expensive) 100 MHz OCXO was put in place of the TCXOs. An internal divider on the XA/XB input was enabled to divide the input by two so that the same ClockBuilder-Pro project file could be used.

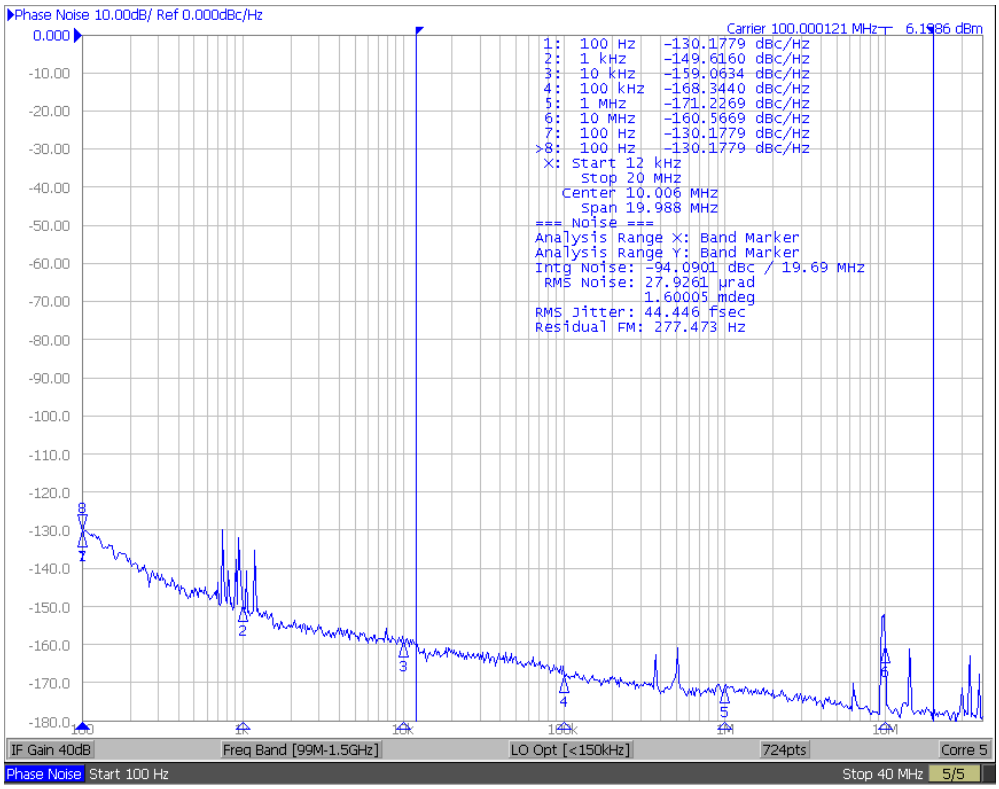

Figure 7.1. 100 MHz OCXO

Although the OCXO has some spurs, overall its phase noise is extremely low.

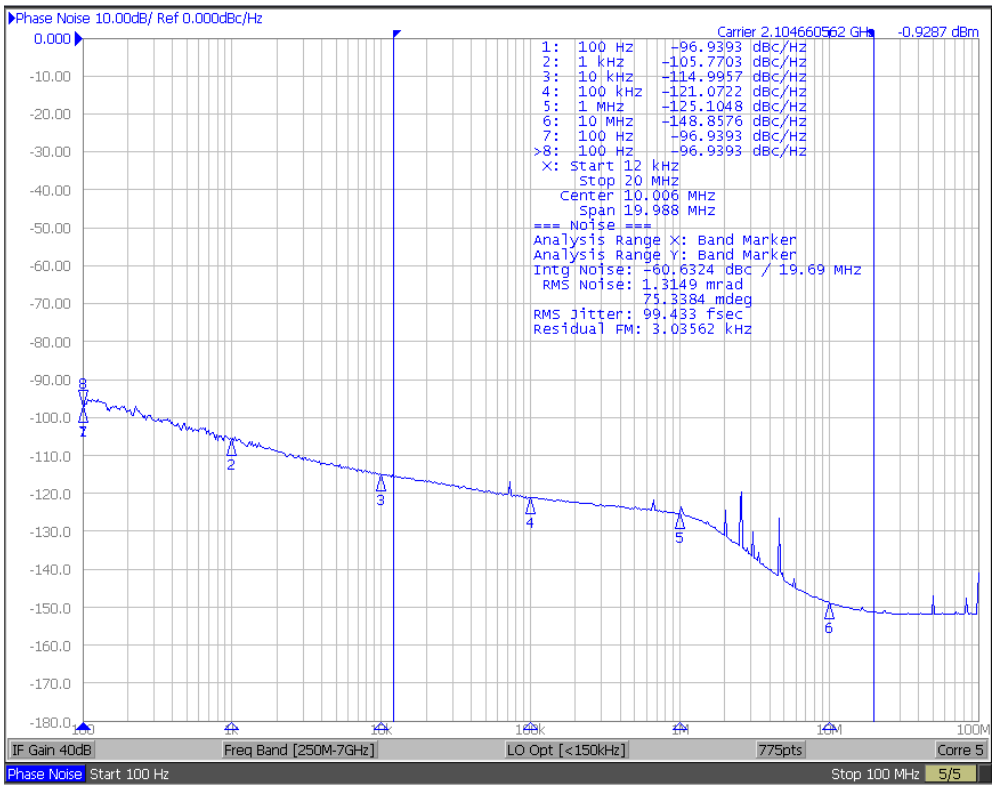

Figure 7.2. Si5344H with a High Performance OCXO

The low phase noise of the OCXO helps to improve Si5344H performance. This level of performance is similar to what one would expect when using a crystal at the XAXB pins (see Figure 1.1 Crystal Resonator Connection on page 2).

8. RMS Jitter Value Tables

The following tables list the jitter values from the phase noise plots provided in this application note.

Table 8.1. TCXO/OCXO Jitter Values in fsec RMS from the Phase Noise Plots

Figure	Jitter
Figure 4.2 TCXO A with 100 nf on page 8	560
Figure 4.3 TCXO B with Just 100 nf on page 8	872
Figure 5.1 TCXO A with Added 100 µf Cap on page 10	346
Figure 5.2 TCXO B with Added 100 uf cap on page 10	374
Figure 6.1 TCXO A using the E5052B Power Supply on page 12	293
Figure 6.2 TCXO B using the E5052B Power Supply on page 13	282
Figure 7.1 100 MHz High Performance OCXO on page 15	44

Table 8.2. Si5344H Jitter Values from the Phase Noise Plots

Figure	Jitter
Figure 4.4 Si5344H with TXCO A and Just a 100 nf Cap on page 9	202
Figure 4.5 Si5344H with TCXO B and a 100 nf Cap on page 9	172
Figure 5.3 Si5344H using TCXO A with Added 100 µf Cap on page 11	163
Figure 5.4 Si5344H using TCXO B with Added 100 µf Cap on page 11	160
Figure 6.1 TCXO A using the E5052B Power Supply on page 12	146
Figure 6.4 Si5344H with TCXO B and the E5052B Power Supply on page 14	147
Figure 7.2 Si5344H with a High Performance OCXO on page 16	99

9. Conclusions

When using oscillators as the reference input to the XAXB pins on Si5342-47, care must be taken with regard to the following issues:

1. If the oscillator cannot drive a 50 Ω transmission line, it must be located as close to the Si534x as possible to eliminate transmission line effects.
2. The DC load on the output of an oscillator should be considered. Typical TCXOs require 10 kΩ or higher.
3. Because the oscillator signal needs to be attenuated before being connected to the XA pin, care must be taken in designing the attenuator.
4. A typical oscillator such as a TCXO needs a very clean and well-bypassed power supply. For the highest performance, a three-terminal, linear regulator should be considered. There are significant variations in the output noise of three-terminal regulators, so a low noise regulator should be chosen for the best performance. To avoid additional stray noise pickup, this regulator should ideally supply power only to the TCXO.
5. An exceptionally clean XA/XB signal results in very low jitter, similar to the jitter that one would expect when using a crystal as the XA/XB source. However, an uncompensated crystal results in high wander generation, particularly with loop bandwidths below ~40Hz. For applications that need both the lowest jitter and wander, consider using an Si5348, Si5383, or Si5384. These devices provide a true “best of both worlds” solution.

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