AN1035: Timing Solutions for 12G-SDI

Digital Video technology is ever-evolving to provide higher quality, higher resolution video imagery for richer and more immersive viewing experiences. Ultra-HD/4K digital video systems have now become mainstream. In support of this trend, broadcast video systems from camera, through editing, production, and distribution equipment to end viewing devices, all require accelerated digital video processing and higher speed transport capability. Behind much of this underlying technology is an organization called SMPTE (Society of Motion Picture and Television Engineers, www.smpte.org) whose charter is to advance the art and science of bringing high quality, motion imaging content to the world. SMPTE has developed many leading edge imaging equipment standards, including the 12G-SDI high speed digital video transport standard. These standards were developed to assist manufacturers of digital video equipment in the design of interoperable high-performance video systems.

This application note will primarily focus on 12G-SDI physical layer reference clock timing requirements for implementations of SMPTE ST-2082 (12G spec). The ST-2082 standard specifies operation of high bandwidth serial digital & audio transport protocols over 75 Ω coax. (In general, if reference clock performance can support 12G-SDI, it can also easily support 6G-SDI.) For an overview of legacy video transport standards (3G and earlier), refer to *AN377: Timing and Synchronization in Broadcast Video*. Application note AN377 contains information on legacy digital video transport standards and an overview of various common video system components.

KEY POINTS

- 12G-SDI physical layer reference clock timing requirements for implementations of SMPTE ST-2082 (12G spec)
- ST-2082 standard specifies operation of high bandwidth serial digital & audio transport protocols over 75 Ω coax

1. Applications supporting 12G-SDI

Below are a few applications examples of digital video system components that may require 12G-SDI support. As you can see from this list, 12G-SDI has the potential to be quite prolific.

- Format Converters/Routers/Servers
- Switchers/Editing/Replay Systems
- Production/Post Systems
- Professional Cameras/Displays

Designers and manufacturers of equipment for digital video systems supporting 12G-SDI have two basic choices when selecting 12G-SDI Integrated Circuit (IC) devices.

The first choice is standard, off-the-shelf purpose-built 12G-SDI IC devices that implement the specific digital video transport function typically required in digital video systems. This approach usually requires additional external devices to implement additional digital video processing features beyond video transport. Many systems will utilize FPGA devices to implement the additional video processing as a FPGA-assisted architecture.

The second choice is to utilize a FPGA device that can handle both the 12G-SDI digital video transport function as well as implement additional digital video processing features. This is an FPGA-centric architecture.

Many digital video system architects choose either a FPGA-assisted or FPGA-centric approach. In either case, FPGAs have become a central component of 12G-SDI based systems. Meeting the FPGA's 12G-SDI reference clock timing requirements has now become a central design concern and is addressed in this application note.

2. 12G-SDI Timing Requirements in FPGAs

The same reference clock frequencies that are used in many 3G and earlier systems may also be found in 6G and 12G based systems. An example of some of the familiar reference clock frequencies are as follows:

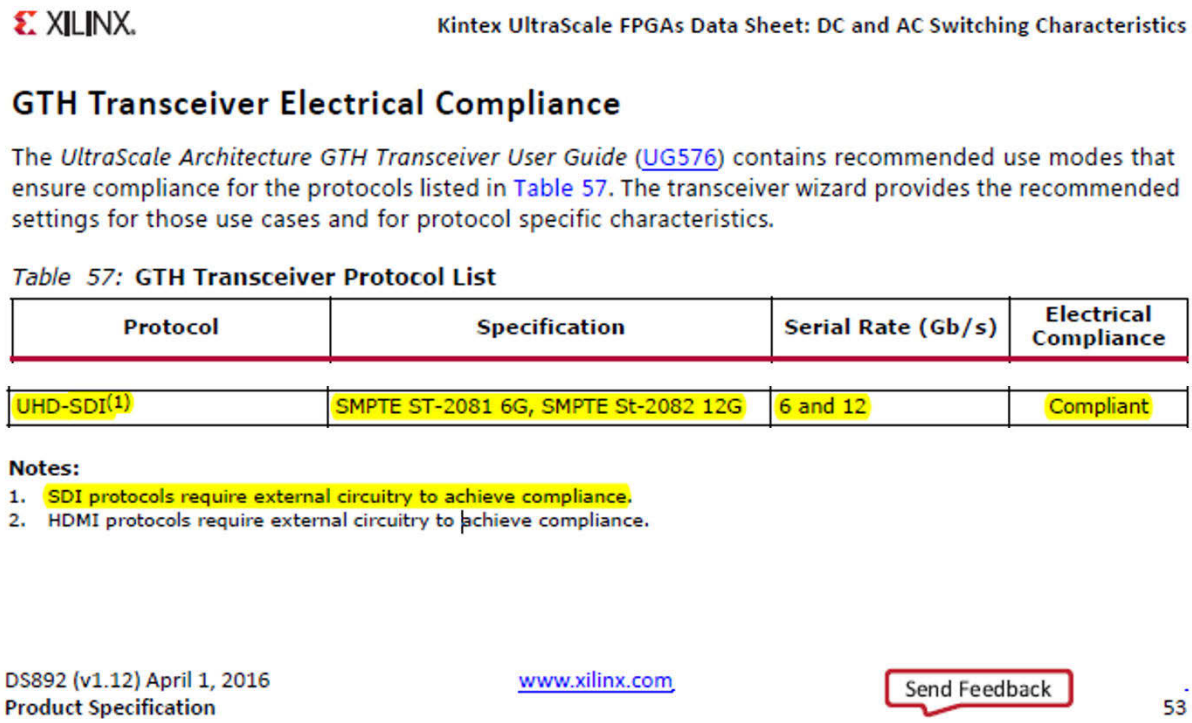
- 74.25 MHz, 74.25 MHz/1.001
- 148.5 MHz, and 148.5 MHz/1.001
- 297.0 MHz and 297.0 MHz/1.001

SDI capable FPGAs incorporate transceiver blocks with internal PLLs used to multiply up a reference clock (e.g. 148.5MHz) to the transceiver's required bit rate. For 12G-SDI the physical layer bit rate is 11.88 Gbps, or 80x the reference clock. But, a reference clock of proper frequency alone (i.e. 148.5 MHz) is not good enough to use as a 12G-SDI transceiver transmit reference clock. The reference clock must meet both frequency and jitter requirements. To generate jitter compliant 12G-SDI channels, the internal clock multiplying PLL typically requires a low jitter input reference clock. For most SDI rates, and especially at 12G-SDI rates, the required PLL reference clock jitter requirements are stringent enough to require a clock that is generated outside of the FPGA, away from noise sources internal to a high-speed FPGA. As a result, each FPGA vendor specifies specific jitter requirements of the externally supplied 12G-SDI transceiver reference clock.

The two main FPGA vendors that support 12G-SDI capability are Altera Corporation and Xilinx, Inc. As you will see in the following sections of this application note, the reference clock jitter requirements of Altera and Xilinx FPGAs for 12G-SDI applications can be met by many Silicon Labs devices.

3. Xilinx FPGA UltraScale GTH transceivers are 12G-SDI compliant

The figure below shows an excerpt taken from the Xilinx Kintex UltraScale Data Sheet. It shows the UltraScale GTH transceiver is SMPTE ST-2081 (6G-SDI) and SMPTE ST-2082 (12G-SDI) compliant, but with inclusion of certain required external circuitry. This external circuitry includes a low jitter reference clock source.



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Kintex UltraScale FPGAs Data Sheet: DC and AC Switching Characteristics

GTH Transceiver Electrical Compliance

The *UltraScale Architecture GTH Transceiver User Guide* (UG576) contains recommended use modes that ensure compliance for the protocols listed in Table 57. The transceiver wizard provides the recommended settings for those use cases and for protocol specific characteristics.

Table 57: **GTH Transceiver Protocol List**

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
UHD-SDI(1)	SMPTE ST-2081 6G, SMPTE St-2082 12G	6 and 12	Compliant

Notes:
1. SDI protocols require external circuitry to achieve compliance.
2. HDMI protocols require external circuitry to achieve compliance.

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Figure 3.1. Excerpt from Xilinx Kintex UltraScale Data Sheet

4. Xilinx FPGA 12G-SDI Reference Clock Performance Requirements

A useful guide for designers implementing 12G-SDI in Xilinx UltraScale devices is Xilinx document XAPP1248 entitled “Implementing SMPTE SDI Interfaces with UltraScale GTH Transceivers”. Below is an excerpt taken from this Xilinx application note on reference clock implementation for SMPTE SDI interfaces using their UltraScale GTH transceiver. Note the reference clock sources shown at the bottom of the Xilinx Figure 1 block diagram. This external reference clock source must have the ability to generate both a Base frequency clock and Base frequency/1.001 clock simultaneously. As indicated in this Xilinx document, the clock source can either be free-running or must be locked to another clock source (e.g., Genlock or locked to Rx clock), depending on the intended SDI system application. An example of a free-running but variable frequency clock source is a stand-alone clock generator (e.g., Silicon Labs Si5340/41). For those applications requiring lock to a studio timing source (Genlock), or locking to and cleaning a jittery clock (using Rx clock), a jitter attenuator that can perform synchronization and/or jitter reduction (e.g., Si5342/44/45 family) is required. Note that the Base frequency of this source may need to change depending on SDI interface requirements. Xilinx suggested reference clocks are 148.5 MHz and 148.5 MHz/1.001 and the ability to generate both simultaneously is important, specifically for 12G-SDI functionality in Xilinx GTH transceivers.

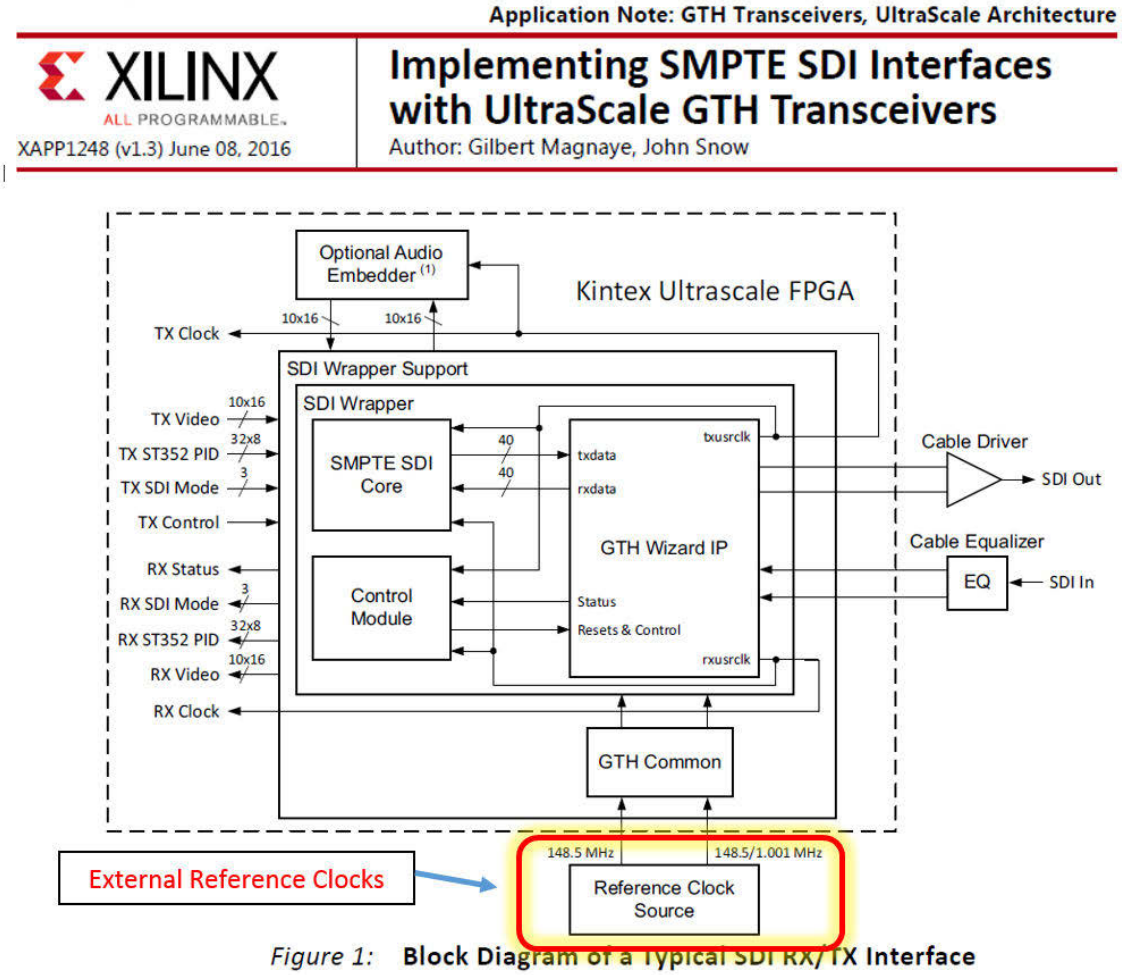

Figure 4.1. Excerpt from Xilinx UltraScale SMPTE SDI Interface Application Note - XAPP1248

In addition to frequency flexibility, the Xilinx external reference clocks must also meet certain jitter performance criteria in order for the GTH transceiver to meet the jitter performance of the 12G-SDI channel. The required reference clock jitter performance is typically specified in terms of maximum phase noise over certain offset frequency ranges. (The offset frequencies ranges specified are derived from a combination of end protocol requirements and internal PLL characteristics with the goal of ensuring the end protocol specifications are met.) The resulting maximum phase noise profile is called a phase noise mask since it specifies the maximum allowable phase noise over certain frequencies. Compliant reference clocks must have a phase noise profile below these limits. Xilinx specifies the GTH reference clock phase noise mask in both the Kintex and Virtex UltraScale data sheets as shown below.

Table 52: **GTH Transceiver Reference Clock Selection Phase Noise Mask**

Symbol	Description	Offset Frequency	Min	Typ	Max	Units
$QPLL_{REFCLKMASK}$ (1)(2)	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 KHz	–	–	–105	dBc/Hz
		100 KHz	–	–	–124	
		1 MHz	–	–	–130	
$CPLL_{REFCLKMASK}$ (1)(2)	CPLL reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 KHz	–	–	–105	dBc/Hz
		100 KHz	–	–	–124	
		1 MHz	–	–	–130	
		50 MHz	–	–	–140	

Notes:

1. For reference clock frequencies other than 312.5 MHz, adjust the phase-noise mask values by 20 x Log(N/312.5) where N is the new reference clock frequency in MHz.
2. This reference clock phase-noise mask is superseded by any reference clock phase-noise mask that is specified in a supported protocol, e.g., PCIe.

Figure 4.2. Excerpt from Xilinx Kintex UltraScale Data Sheet

In Xilinx Table 52 above, the phase noise mask is based on a clock (carrier) frequency of 312.5 MHz. We need phase noise levels referenced to 148.5 MHz. Since phase noise scales with frequency, we need to scale the data sheet values for equivalent phase noise at the required frequency of 148.5 MHz. This well-known equation for frequency scaling is given in footnote 1 of Xilinx Table 52 shown above. The table below shows the new phase noise mask levels after the required frequency scaling equation is applied.

Table 4.1. Phase Noise Frequency Scaling for 148.5 MHz

	Data sheet Ref Freq	Scaled for 12G-SDI Ref Freq
	3.125E+08	1.485E+08
Offset (Hz)	**Ref Level (dBc/Hz)**	**New Level (dBc/Hz)**
1.00E+04	-105	-111.5
1.00E+05	-124	-130.5
1.00E+06	-130	-136.5
5.00E+07	-140	-146.5

Now that we have the phase noise mask scaled for the required 148.5 MHz reference clock frequency for 12G-SDI, let's see how the Si5345 (Jitter Attenuator) and Si5341 (Clock Generator) perform relative to the Xilinx required phase noise mask.

Below are actual phase noise plots of a Si5345 jitter attenuator and Si5341 clock generator (in blue) with Xilinx phase noise mask superimposed (in red). As you can see, both the Si5345 and Si5341 easily meet the Xilinx 12G-SDI phase noise requirements.

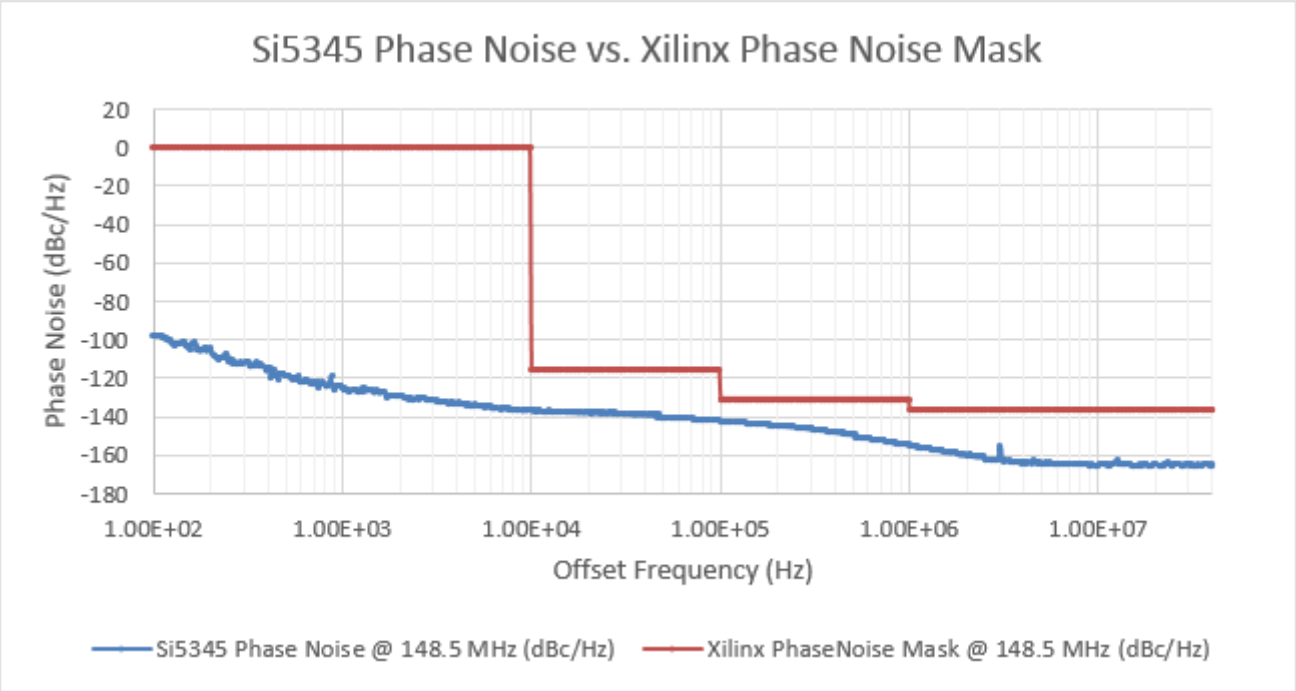

Figure 4.3. Si5345 Phase Noise vs. Xilinx Phase Noise Mask

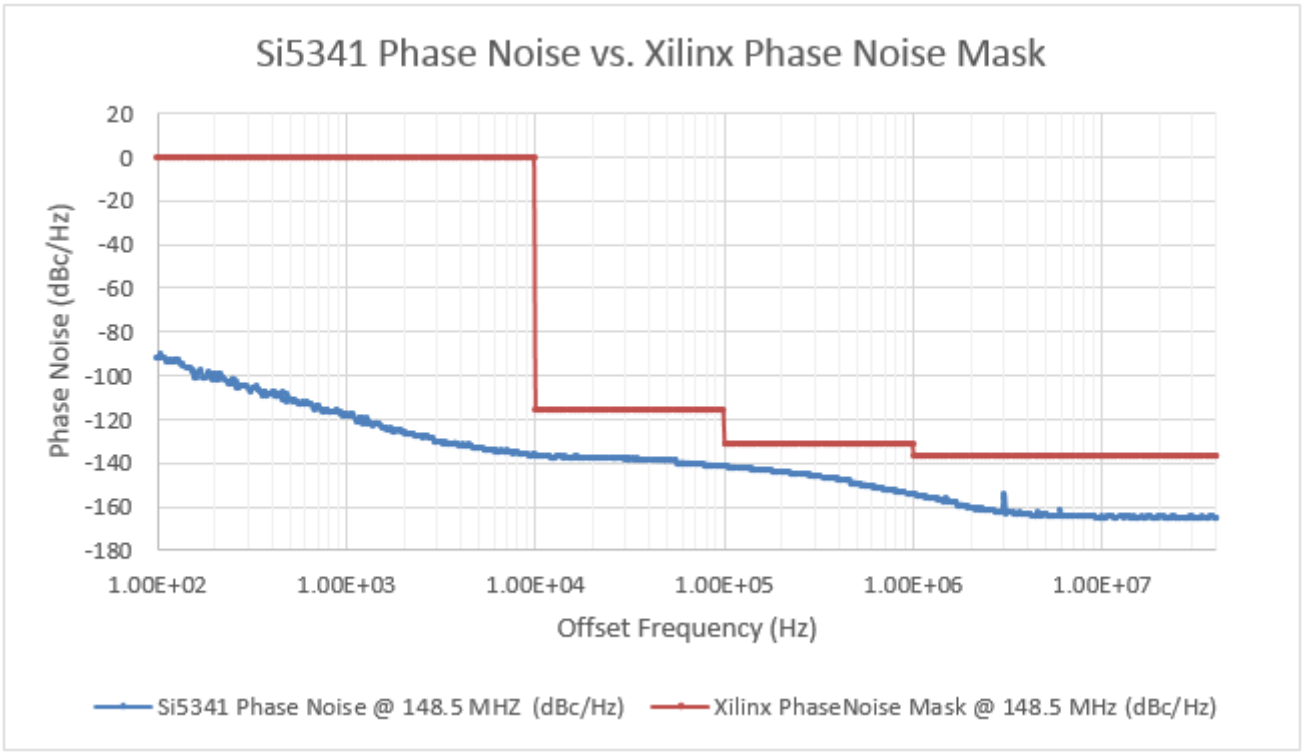

Figure 4.4. Si5341 Phase Noise vs. Xilinx Phase Noise Mask

5. Altera Arria 10 FPGA Supports 12G-SDI

Let's now shift focus to Altera 12G-SDI implementations. The table below was taken from Altera's "SDI II IP Core User Guide", UG-01125. This document shows the Arria 10 is required for 12G-SDI support.

Table 2-1: SDI Standard Support

Table below lists the SDI standard support for various FPGA devices.

Device Family	SDI Standard						
	Single Standard				Multiple Standards		
	SD-SDI	HD-SDI	3G-SDI	Dual Link HD-SDI	Dual Standard (up to HD)	Triple Standard (up to 3G)	Multi Standard (up to 12G)
Arria V GX	Yes	Yes	Yes	Yes	Yes	Yes	No
Arria V GZ	Yes	Yes	Yes	Yes	Yes	Yes	No
Stratix V	Yes	Yes	Yes	Yes	Yes	Yes	No
Cyclone V	Yes	Yes	Yes	Yes	Yes	Yes	No
Arria 10	No	Yes	Yes	Yes	No	Yes	Yes

Figure 5.1. Excerpt from Altera 'SDI II IP Core User Guide' Showing 12G-SDI Supported Device Family

6. Altera FPGA 12G-SDI Reference Clock Performance Requirements

For best performance, Altera recommends using external reference clocks. Below is an excerpt from the Altera "Arria 10 Transceiver PHY User's Guide"

Input Reference Clock Sources

The transmitter PLL and the clock data recovery (CDR) block need an input reference clock source to generate the clocks required for transceiver operation. The input reference clock must be stable and free-running at device power-up for proper PLL calibrations.

Arria 10 transceiver PLLs have five possible input reference clock sources, depending on jitter requirements:

- Dedicated reference clock pins
- Reference clock network
- The output of another fPLL with PLL cascading (46)
- Receiver input pins
- Global clock or core clock (46)

(46) Not available for CMU

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Dedicated Reference Clock Pins 3-29

Altera recommends using the dedicated reference clock pins and the reference clock network for the best jitter performance.

Figure 6.1. Excerpt from Altera "Arria 10 Transceiver PHY User's Guide" Showing Clock Source Recommendation

The information above tells us that Altera recommends using an external device, like the Si5340/41 clock generator or Si5342/44/45 Jitter attenuating clock generator for best (lowest) jitter performance. Since 12G-SDI is a higher bit rate protocol, low jitter is especially important for reliable and robust operation.

The Arria 10 data sheet excerpt below specifies the reference clock phase noise mask requirements, shown highlighted, for all supported Arria 10 transceivers. Note the phase noise mask table specification is referenced to 622 MHz and will require frequency scaling to determine the phase noise mask for the specific 12G-SDI reference frequency needed.

Symbol/Description	Condition	Transceiver Speed Grades 1, 2, 3, 4, and 5			Unit
		Min	Typ	Max	
Transmitter REFCLK Phase Noise (622 MHz) (37)	100 Hz	—	—	–70	dBc/Hz
	1 kHz	—	—	–90	dBc/Hz
	10 kHz	—	—	–100	dBc/Hz
	100 kHz	—	—	–110	dBc/Hz
	≥ 1 MHz	—	—	–120	dBc/Hz
Transmitter REFCLK Phase Jitter (100 MHz)	1.5 to 100 MHz (PCIe)	—	—	4.2	ps (rms)
R_{REF}	—	—	2.0 k ±1%	—	Ω
$T_{SSC-MAX-PERIOD-SLEW}$	Max SSC df/dt			0.75	

Figure 6.2. Excerpt from Altera "Arria 10 Transceiver Data Sheet" Showing Reference Clock Phase Noise Mask

For purposes of this application note, 148.5 MHz will be chosen for the Altera 12G-SDI reference frequency. Below is a table of the resulting scaled phase noise mask.

Table 6.1. Altera Arria 10 Phase Noise Mash Frequency Scaling

	Data sheet Ref Freq	Scaled for 12G-SDI Ref Freq
	6.22E+08	1.485E+08
Offset (Hz)	**Ref Level (dBc/Hz)**	**New Level (dBc/Hz)**
1.00E+02	-70	-82.4
1.00E+03	-90	-102.4
1.00E+04	-100	-112.4
1.00E+05	-110	-122.4
1.00E+06	-120	-132.4

Using the scaled phase noise mask at 12G-SDI 148.5 MHz reference clock frequency, let's see how the Si5345 (Jitter Attenuator) and Si5341 (Clock Generator) performs relative to the Altera required phase noise mask.

Below are actual phase noise plots of a Si5345 jitter attenuator and Si5341 clock generator with Altera phase noise mask superimposed. As you can see, both the Si5345 and Si5341 easily meet the Altera 12G-SDI phase noise requirements.

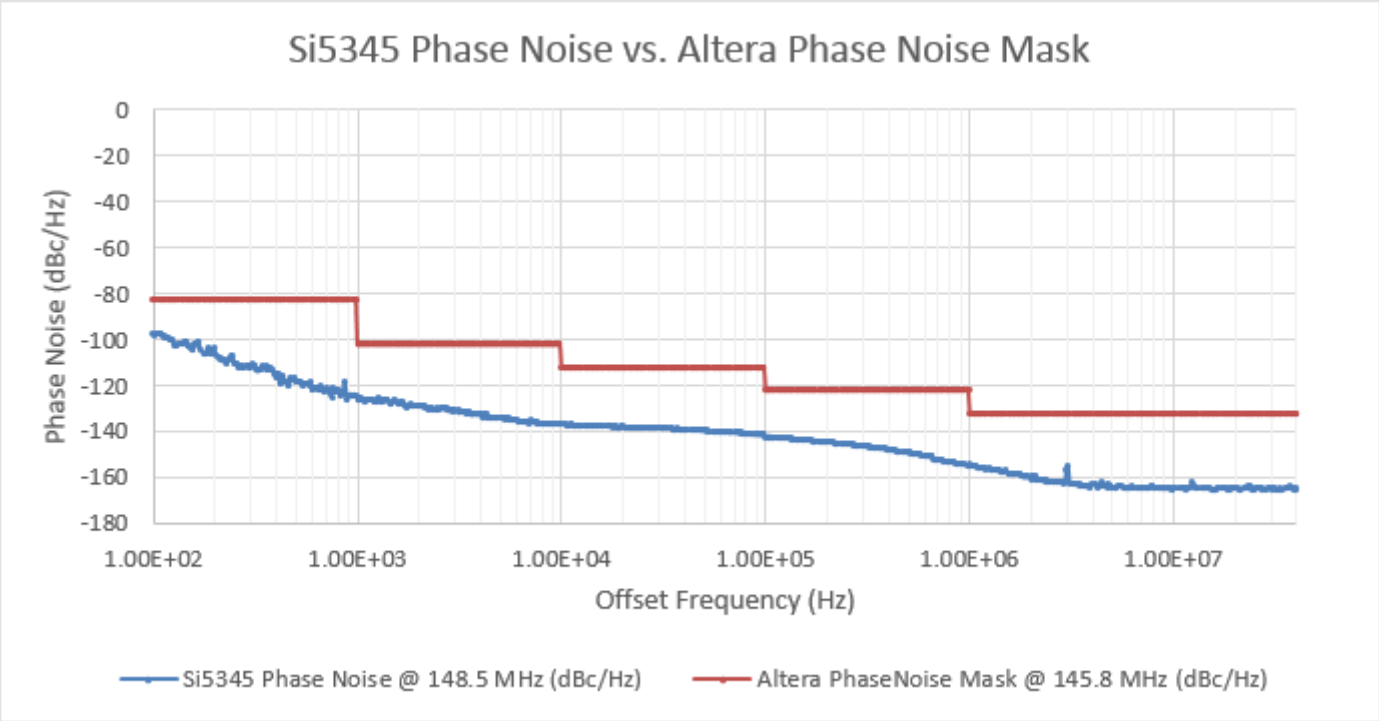


Figure 6.3. Si5345 Phase Noise vs. Altera Phase Noise Mask

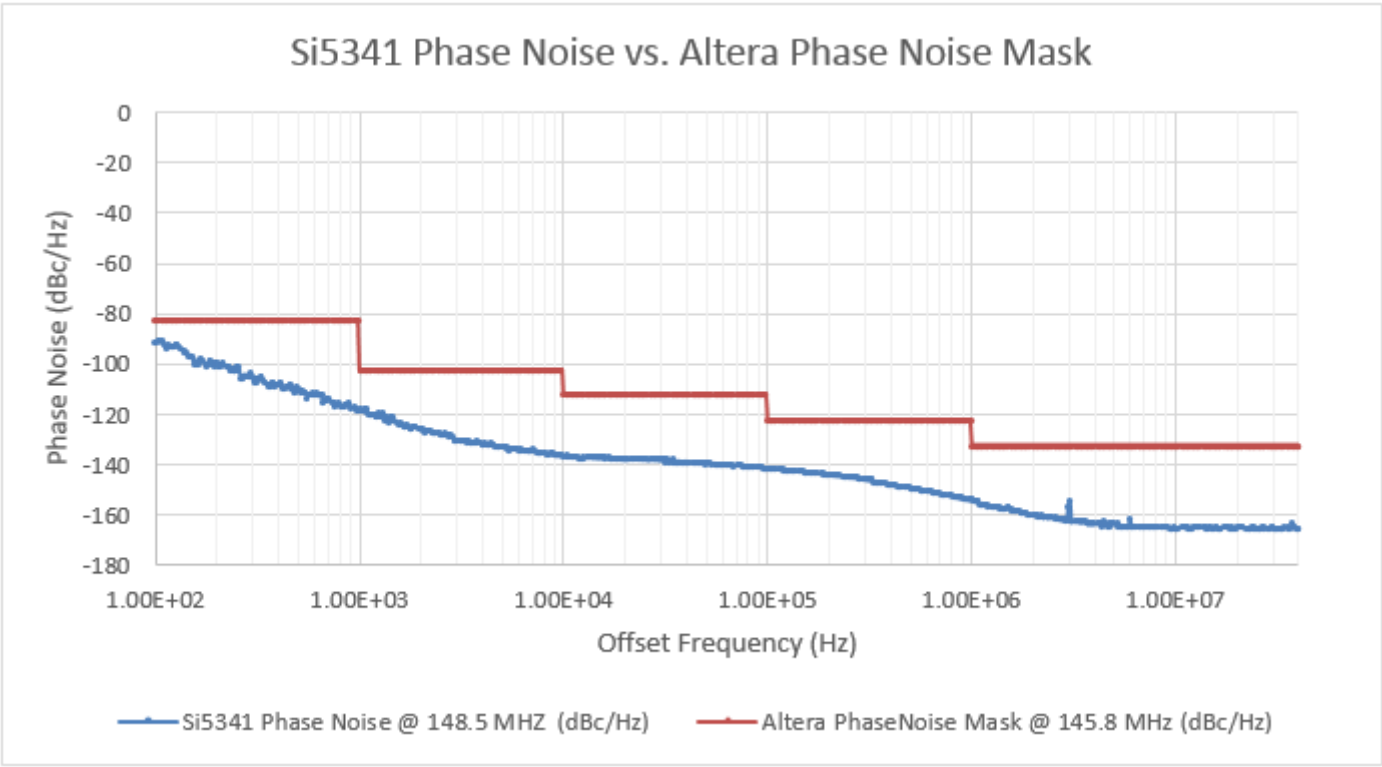


Figure 6.4. Si5341 Phase Noise vs. Altera Phase Noise Mask

7. Alternate Altera 12G-SDI Reference Clock Phase Noise Mask

There is an alternate phase noise mask Altera may recommend for certain 12G-SDI applications requiring a reference clock at 297 MHz. (Contact Altera directly for more details on this 12G-SDI alternate phase noise mask.) Below are phase noise plots for both Si5341 and Si5345 versus the alternate 297 MHz mask. The Si5345 and Si5341 comply with this mask as well.

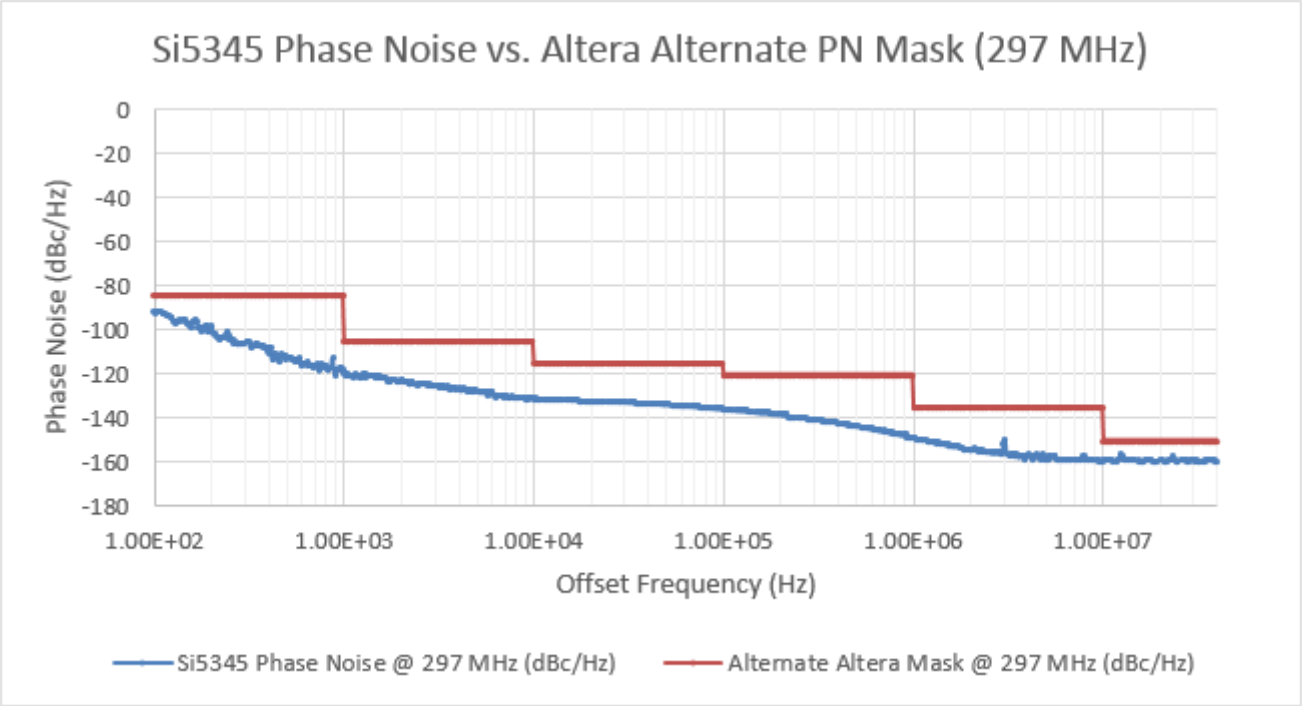


Figure 7.1. Si5345 Phase Noise vs. Altera Alternate Phase Noise Mask

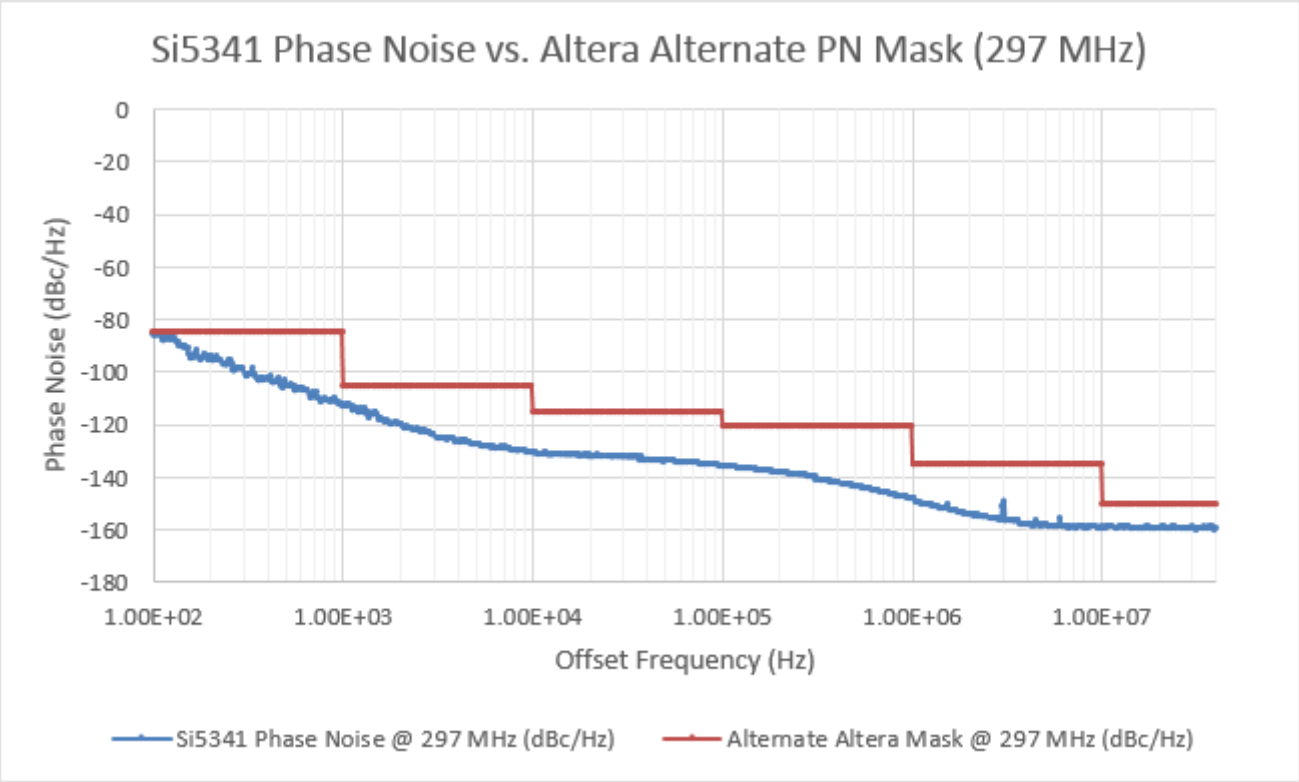


Figure 7.2. Si5341 Phase Noise vs. Altera Alternate Phase Noise Mask

8. Optimized 12G-SDI Clocking Architecture using Si5345

The figure below is an example block diagram of legacy SDI clocking architecture used in some existing FPGA implementations. This architecture generates the video and audio clocks required by 12G-SDI systems but is inefficient in terms of number of devices, power consumption, and flexibility. The clock generator in this architecture produces the required video/audio clocks, but requires additional external components that add cost and limit configuration flexibility. Also, this architecture requires additional components to generate general system clocks.

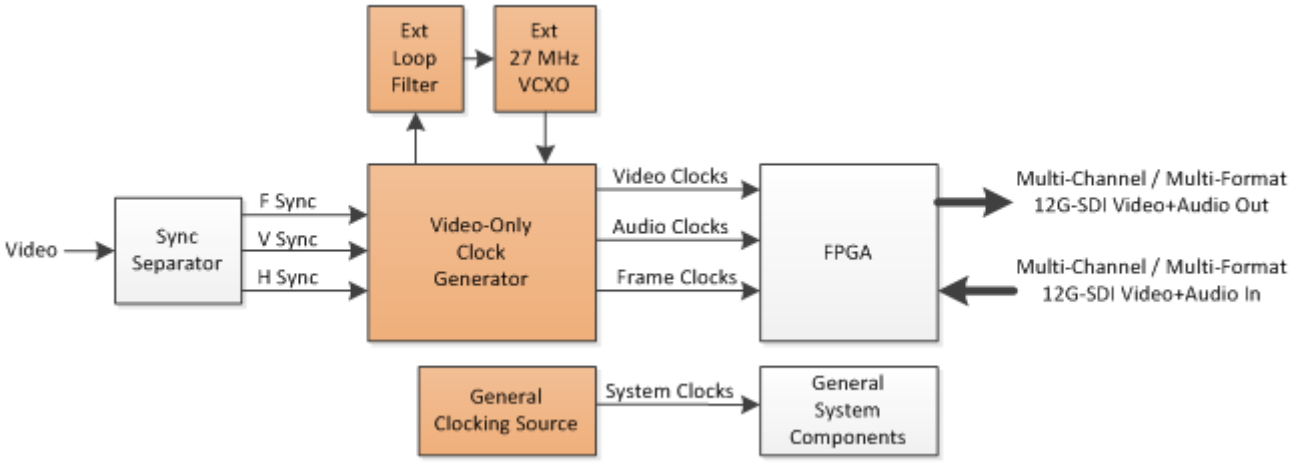


Figure 8.1. Legacy SDI/HD-SDI/12G-SDI Clocking Architecture

The figure below shows an example of an optimized architecture that reduces device count while adding configuration flexibility by utilizing the Si5345 along with a small amount of existing FPGA resources. Notice in this architecture no external components are required for the Si5345. Also, additional general system clocks can be generated by Si5345 along with the required video/audio clocks. This optimized architecture greatly simplifies the overall system clocking design. The Si5345 configuration, including frequencies, output assignments, and loop bandwidths, can be changed via I2C commands from the FPGA making this architecture very flexible and reusable across many different systems and products.

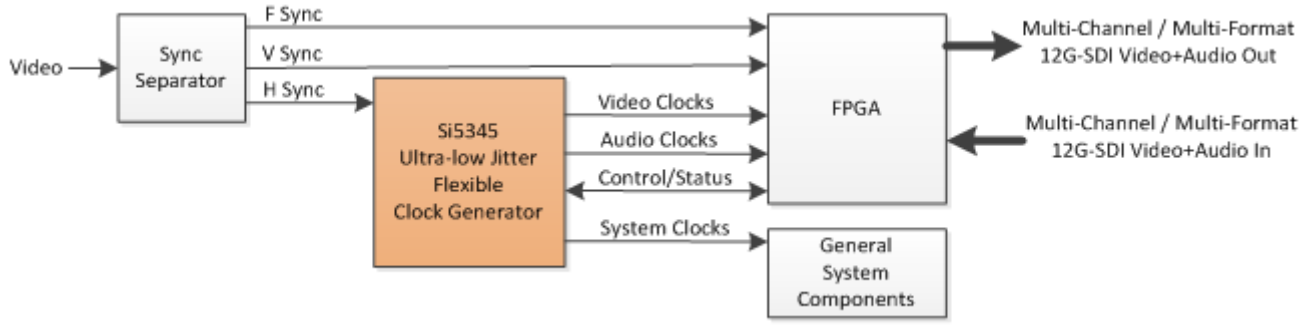


Figure 8.2. Optimized SDI/HD-SDI/12G-SDI Clocking Architecture w/Si5345

9. Leveraging Existing SDI Clock Architectures for 12G-SDI

In some instances it may be desirable to use existing SDI product architectures and simply attempt to extend support to include 12G-SDI capability. Many of these legacy products may use VCXOs (Voltage Controlled Crystal Oscillators), simple XOs (Crystal Oscillators), or perhaps even pin or I2C controlled XOs. Several Silicon Labs' VCXO/XO clocking devices can support 12G-SDI jitter requirements and meet the phase noise masks already mentioned in this application note.

Below is a table showing 3G, 6G, and 12G-SDI standards along with Silicon Labs clock devices that can be used to potentially support these standards. Of course when considering leveraging an existing product architecture and its potential to support a higher performance standard, all areas of that architecture must be examined, including clock performance requirements. This table serves as a guide to timing product families and is not meant to suggest legacy SDI products can be upgraded by simply changing or upgrading clocking devices.

Table 9.1. Silicon Labs Clock Devices vs. SMPTE Standards & FPGAs

FPGA Specs						Silicon Labs Clock Devices			
Vendor	Series	SMPTE Standard(s)	Vendor IP	Reference Clock (MHz)	RMS Phase Jitter (12 KHz - 20 MHz)	Clock Gen	JA Clock	XO/VCXO	RMS Phase Jitter (12 KHz - 20 MHz)
Altera	Arria 10	12G-SDI 6G-SDI 3G-SDI	SDI II IP Core	297 297/1.001	0.43 ps	Si5340/41	Si5342/4/5	Si53x, Si57x, Si54x[1], Si56x[1]	0.1 - 0.3 ps
	Arria V GX, GZ, Stratix V, Cyclone V	3G-SDI		148.5 148.5/1.001	0.90 ps	Si5335/38 Si5340/41	Si5342/4/5	Si59x, Si53x, Si55x, Si57x	0.1 - 0.7 ps
Xilinx	Kintex & Virtex UltraScale GTH	12G-SDI 6G-SDI 3G-SDI	LogiCORE IP SMPTE UHD-SDI Core	148.5 148.5/1.001	0.71 ps	Si5335/38 Si5340/41	Si5342/4/5	Si53x, Si55x, Si57x, Si54x[1], Si56x[1]	0.1 - 0.5 ps
	Kintex-7 GTX, Virtex 7 GTX	6G-SDI 3G-SDI		148.5 148.5/1.001	0.71 ps	Si5335/38 Si5340/41	Si5342/4/5	Si59x, Si53x, Si55x, Si57x, Si54x[1], Si56x[1]	0.1 - 0.5 ps

Note:
1. Future devices on product roadmap.

Some legacy clocking architectures may use multiple discrete XOs with a clock multiplexer for selection of different frequencies. These applications may be better served by use of a single, multi-frequency, high performance crystal oscillator or VCXO to provide flexibility of selecting different reference clocks in a single device. The Si534 Quad Frequency Crystal Oscillator is an example of a device that can generate up to four different clock frequencies from a single industry standard 5 x 7 mm package. Frequency selection pins (FSel) are used to determine the frequency of the output clock. Several devices in the Si53x and Si54x/6x family are capable of supporting single, dual, or quad frequency options by pin selection or any desired frequency via I2C commands.

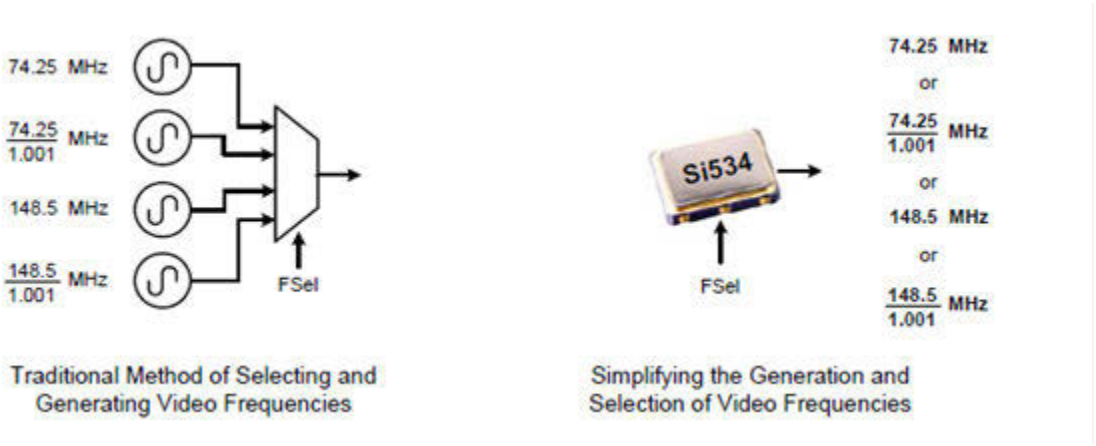


Figure 9.1. Silicon Labs Multi-Frequency Clock Devices Simplify Designs

10. Conclusion

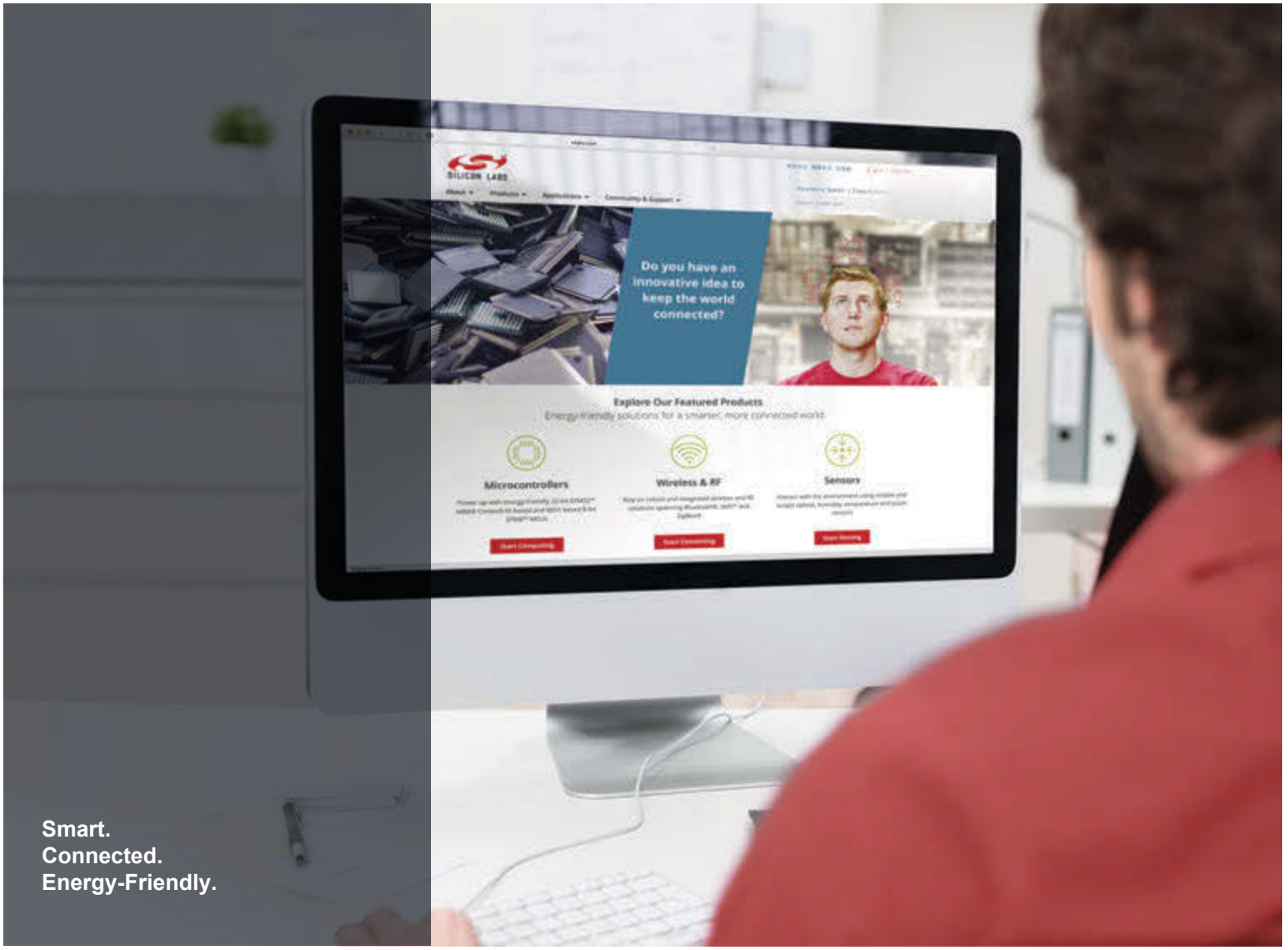
Silicon Labs has several 12G-SDI reference clock timing solutions that meet the 12G-SDI reference clock jitter and frequency requirements for both Altera and Xilinx FPGAs. The devices highlighted in this application note are 4th generation ultra-low jitter clock generator and jitter attenuators that have multiple, independent outputs with flexible output driver format configurations.

The Si534x class of devices have the performance to supply both the low jitter clocks needed for 12G-SDI as well as other system clocks in a single device, minimizing device count and board area. Both the Si5340/41 clock generator family and Si5342/44/45 jitter attenuator family of devices have many other features, including in-system re-configurability, dynamic feature changes via I2C/SPI and are recommended for new designs. The Si5342/44/45 family of jitter attenuating devices have additional features like automatic redundant clock switching, clock holdover in event of total input clock loss, and PLL bandwidth changes by simple I2C commands without requiring ***any*** external components or component changes.

For upgrading of existing products to expand into new applications, or for new designs that require simpler clock tree architectures, consider using devices from our high-performance and flexible XO/VCXO portfolio.

For more information on these high performance and flexible devices, please browse to the following links:

Si5340/41 Clock Generator:	https://www.silabs.com/Support%20Documents/TechnicalDocs/Si5341-40.pdf
Si5342/44/45 Jitter Attenuating Clock:	https://www.silabs.com/Support%20Documents/TechnicalDocs/Si5345-44-42.pdf
Si5xx All Oscillator (XO/VCXO) Products:	http://www.silabs.com/products/clocksoscillators/Oscillators/Pages/default.aspx
Overview of Complete Timing Product Portfolio:	http://www.silabs.com/products/timing/Pages/clocks-buffers-oscillators.aspx



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