AN1006: Differences Between Si534x/8x Revision B and Revision D Silicon

This document highlights differences between Revision B and Revision D silicon for the following part numbers:

- Si5340
- Si5341
- Si5342
- Si5344
- Si5345
- Si5346
- Si5347
- Si5348
- Si5380

SUMMARY

Compared to Revision B, Revision D silicon for Si534x/8x fixes several errata, supports higher maximum output frequency ranges, and offers several new features. This document outlines those differences.

1. Migration from Si534x/8x Revision B to Revision D

Applies to Si5380/48/47/46/45/44/42/41/40

With the release of Revision D for Si534x/8x, the Revision B devices are now classified as "Not Recommended for New Designs" (NRND). As of the Revision D release date, Silicon Labs has no plans to EOL the Si5348/47/46/45/44/42/41/40 Revision B devices and will continue production of both the Revision B devices and the newer Revision D devices. As of the Revision D release date, Silicon Labs does not plan to continue production of Si5380 Revision B devices. Customers using Si5380 must follow the instructions below to migrate their existing Revision B designs to Revision D.

Revision D devices are pin-compatible and footprint-compatible with Revision B devices. However, Revision D devices are not intended to be drop-in replacements for Revision B devices. As a result of changes to the circuitry in Revision D devices, their performance and behavior will not completely match that of Revision B.

- Customers currently using Si5348/47/46/45/44/42/41/40 Revision B in production may continue to do so. Silicon Labs will maintain production of both Revision B and Revision D concurrently.
- Customers who wish to migrate a design from Revision B to Revision D should download the latest version of ClockBuilder Pro and create a new custom OPN for Revision D with their desired configuration. Once a new Revision D OPN has been created, customers should verify functionality of the device in their system prior to starting production with Revision D.
- Silicon Labs does not recommend writing a register file, settings file, or regmap that was created for Revision B to a Revision D device. When migrating an existing design from Revision B to Revision D, customers should download the latest version of ClockBuilder Pro and create new register files, settings files, or regmap exports to be used with Revision D.

1.1 Device Ordering and Identification

Applies to Si5380/48/47/46/45/44/42/41/40

The revision letter which is the 9th digit of the ordering part number indicates "D" for product Revision D. For example: Si5345A-D-GM or Si5345-Dxxxxx-GM, where xxxxx is the custom OPN ID, and D refers to the product revision.

1.2 Evaluation Boards Ordering and Identification

Applies to Si5380/48/47/46/45/44/42/41/40

New evaluation boards are available for all Revision D devices. The Revision D evaluation boards are identified with "-D" in the 7th and 8th characters of the OPN. For example, the Si5345 Revision D OPN is Si5345-D-EVB.

1.3 Handling Revisions in ClockBuilder Pro

ClockBuilder Pro (CBPro) version 2.9 or later supports both Revision B and Revision D of Si534x/8x. Selection of the target device revision is done in Step 2 of the configuration Wizard:

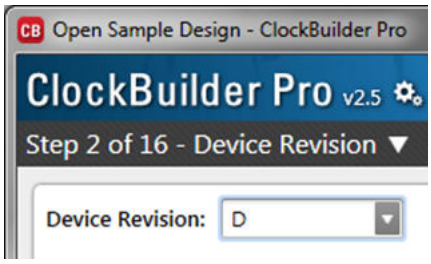

Figure 1.1. Device Revision D

The default revision is "D" for all newly created designs.

CBPro stores the target device revision for each project in the .slabtimeproj project file. When an existing project file is opened, CBPro will set the target device revision according to the data stored in the project file.

With the NRND classification of Si534x/8x Revision D, CBPro will no longer support creation of new custom ordering part numbers (OPNs) for Revision B. Customers with an ongoing Revision B design who still wish to create custom OPNs for Revision B should contact Silicon Labs.

1.4 Changing the Target Device Revision for an Existing CBPro Project

At any time the target device revision for a project can be changed in CBPro by choosing Step 2 "Revision" and then selecting the new target revision from the drop-down box at the top of the screen. Customers who have created projects for Revision B in an earlier version of CBPro can migrate their projects to Revision D using the following steps:

- Open the original project file in CBPro (CBPro will default to Revision B after opening the file.).
- Choose Step 2: "Revision" and select device revision D.
- Click the "Finish" button on the lower right side of the screen.

When changing a project from Revision B to Revision D in CBPro, note the following:

- CBPro will select the default values for any new registers and features that are present in Revision D but were not present in Revision B. This will enable the new Revision D features described below.
- CBPro will recalculate the frequency plan using the latest algorithm for Revision D. As a result, the internal frequency plan for Revision D may differ from the plan used on a Revision B project file.

Although CBPro will allow the device revision to be changed backwards to Revision D from Revision B, this is not recommended, as Revision D contains several enhancements that are not present on Revision B.

2. Errata Fixes

2.1 Revision B Errata Fixed on Revision D

Revision D silicon of Si534x/8x fixes several errata items that were present on Revision B. Details are given below:

Erratum	Part Numbers Affected	Status on Revision D
When entering holdover mode without valid holdover history data, holdover frequency may not be accurate	Si5348/47/46/45/44/42	Fixed
Inadvertent assertion of LOL during clock switching	Si5348/47/46/45/44/42	Fixed
Possible output frequency transients when switching between clocks of the same nominal frequency	Si5348/47/46/45/44/42	Fixed. Utilizes the new ramp switching feature (below) to make adjustments when input clocks not exactly the same frequency.
Exit from holdover ramp feature is not functional	Si5348/47/46/45/44/42	Fixed
Possible part-per-trillion (ppt) frequency offset	Si5348/47/46/45/44/42	Fixed. On Revision B, CBPro included a workaround to avoid this errata. This workaround is no longer needed for Revision D and has therefore been eliminated.
No individual LOS or OOF sticky status bit may be cleared when any other LOS or OOF alarm is asserted	Si5380/48/47/46/45/44/42/41/40	Fixed. Each LOS sticky status bit can now be cleared individually.
Output-to-output skew between clocks generated from different MultiSynth dividers is not consistent at high junction temperatures	Si5345/44/42/41/40/80	Fixed
Input-to-output clock delay variation is not consistent at high junction temperatures	Si5380/45/44/42	Fixed
SMBus timeout	Si5380/48/47/46/45/44/42/41/40	Fixed. The SMBUS_TIMEOUT register is now fully functional.
After power-up the LOS_XAXB pin may be stuck high	Si5347/46/44/42/40	Fixed

2.2 Revision B Errata Not Fixed on Revision D

The following errata from Revision B of Si534x/8x have NOT been fixed on Revision D silicon:

Erratum	Part Numbers Affected	Revision D Notes
Impedance in LVCMOS high-Z mode is too low	Si5380/48/47/46/45/44/42/41/40	This mode is no longer supported on Revision D and has been removed from the data sheet.
VCO drifts to unknown frequency when holdover is disabled and there are no valid input clocks	Si5380/48/47/46/45/44/42	It is not recommended to disable holdover when no input clocks are present. Reference manuals for each OPN have been updated to indicate this behavior.
Input-to-output clock delay variation is not consistent at high junction temperatures	Si5341/40	This specification has been removed from the data sheets for Si5341/40 Revision D. Customers should use Si5345/44/42 if this specification is important for their design.

2.3 Crystal Drive Level

Applies to: Si5380

In data sheet rev 0.96 for Si5380 Revision B, the maximum crystal drive level was incorrectly specified as 200 µW. This has been updated to 300 µW for the Si5380 Revision D data sheet and will be corrected in a future release of the Si5380 Revision B data sheet. In addition, the list of approved crystals in the Si5380 reference manual has been updated to reflect this change.

3. Extended Output Frequency Ranges

Revision D of Si5345/44/42/41/40 offers higher maximum output frequencies than Revision B. The maximum output frequency for each device is indicated below.

Part Numbers	Revision B Maximum Output Frequency	Revision D Maximum Output Frequency
Si5345/44/42/41/40	• 712.5MHz	• Any Frequency up to 720 MHz • Any Frequency from 733.33 MHz - 800 MHz* • Any Frequency from 825 MHz - 1028 MHz*

Note: Certain limitations apply when output frequencies above 720 MHz are selected. Refer to to the Reference Manual for more information.

4. New Features and Capabilities

A variety of new features and capabilities are available on Si534x/8x Revision D. These are described in the following sections.

4.1 Frequency Ramping on Holdover Exit

Applies to Si5380/48/47/46/45/44/42

When coming out of holdover, Revision D allows for the adjustment of frequency ramp rate. This greatly minimizes phase transients due to frequency drift while in holdover. The frequency ramp rate adjustment occurs regardless of whether the output frequencies are using fractional or integer synthesis. This feature may be enabledd or disabled in CBPro, and a variety of ramp rates are selectable from 0.2 ppm/s to 40,000 ppm/s.

- On Si5380/45/44/42, all outputs will ramp in frequency when the DSPLL is coming out of holdover.
- On a Si5348/47/46, only the outputs that connect to the DSPLL that is coming out of holdover will have a ramp in frequency.

4.2 Frequency Ramping on an Input Clock Switch

Applies to: Si5380/48/47/46/45/44/42

When switching between clock inputs that are not synchronous, Revision D allows for the adjustment of the frequency ramp rate. This greatly minimizes phase transients on the output clocks during the input switching. The frequency ramp rate adjustment occurs regardless of whether the output frequencies are using fractional or integer synthesis. This feature may be enabled or disabled in CBPro, and a variety of ramp rates are selectable from 0.2 ppm/s to 40,000 ppm/s.

- On Si5380/45/44/42, all outputs will ramp in frequency when the input clock is switched.
- On a Si5348/47/46, when a DSPLL input switch occurs, only the outputs that connect to that DSPLL will have a ramp in frequency.

4.3 Holdover Exit Bandwidth Selection

Applies to: Si5380/48/47/46/45/44/42

In Revision D, it is possible to select a PLL bandwidth to be used upon Holdover and Free Run exit. This bandwidth cannot be set to less than the normal bandwidth. The device returns to the normal bandwidth after the PLL has locked.

4.4 Loss of Lock Detector Improvements

Applies to: Si5380/48/47/46/45/44/42/41/40

In Revision D, the Si534x/8x LOL detector has been improved to quickly assert LOL on large changes in ppm. Previously on Revision B, a large input frequency change took much longer to assert LOL. The threshold at which LOL is asserted for large ppm changes is set automatically by CBPro based on the frequency plan, and will range from 100 ppm to 1,000,000 ppm.

The Si534x/8x Revision D LOL detector has also been improved to detect loss of an input clock signal. On Revision D, if an input clock edge is not detected within 417 µs, LOL will be asserted. Previously on Revision B, loss of an input clock would only trigger LOS and not LOL.

4.5 Out of Frequency Detector Improvements

Applies to: Si5380/48/47/46/45/44/42

In Si534x/8x Revision D, the OOF detector has been improved so that OOF is asserted when a loss of signal occurs. Previously on Revision B, the OOF detector would not assert when a loss of signal occurs.

Previously on Revision B, either the fast OOF threshold or the precision OOF threshold could be used to both assert and deassert the OOF signal. With Revision D, if the input frequency exceeds either the fast OOF threshold or the precision OOF threshold, OOF will be asserted. However, the input frequency must fall below both OOF thresholds in order for the OOF detector to be deasserted.

4.6 Reductions in Output Clock Phase Transients

Applies to: Si5380/48/47/46/45/44/42

When performing hitless switching, the output clock phase transient has been reduced in Si534x/8x revision D. New values for this can be found in the data sheet.

Additional circuitry optimizes the switching time between Fastlock and normal bandwidth. This reduces output clock phase transients when changing bandwidths.

5. Changes to Registers from Revision B to Revision D

The majority of registers present in Si534x/8x Revision B have been left unchanged in Revision D. The exceptions to this are documented below.

5.1 Device Revision

Applies to: Si5380/48/47/46/45/44/42/41/40

In Si534x/8x the DEVICE_REV register will now read back 0x03 to indicate Revision D. Previously this read back as 0x01 to indicate Revision B.

5.2 Preamble and Postamble

Applies to: Si5380/48/47/46/45/44/42/41/40

In order to change certain registers that affect PLL lock status it is necessary to write a preamble and postamble sequence to the device. The values for the preamble and postamble sequences have changed for Revision D as shown below.

Table 5.1. Preamble Sequence for Si5380/47/46/45/44/42/41/40

Register	Value in Revision B	Value in Revision D
0x0B24	0xD8	0xC0
0x0B25	0x00	0x00

Table 5.2. Postamble Sequence for Si5380/47/46/45/44/42/41/40

Register	Value in Revision B	Value in Revision D
0x0B24	0xDB	0xC3
0x0B25	0x02	0x02

Table 5.3. Preamble Sequence for Si5348

Register	Value in Revision B	Value in Revision D
0x0B24	0xD8	0xC0
0x0B25	0x04	0x04

Table 5.4. Postamble Sequence for Si5348

Register	Value in Revision B	Value in Revision D
0x0B24	0xDB	0xC3
0x0B25	0x06	0x06

Note that on a Revision D device, either the Revision B values or the Revision D values can be written for the preamble/postamble sequence and the device will function the same in either case. However only the Revision D values can be read back from the device.

5.3 New Registers Present on Revision D

Applies to Si5380/48/47/46/45/44/42/41/40

Several new registers have been added to the Si534x/8x Revision D devices to support the new features described above. Details about these new features can be found in the reference manual for each device.

ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

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